EDA Conversion for Advanced Borescope PCB

Scope: Electronic Design Automation Conversion

Application: Manufacturing Industries

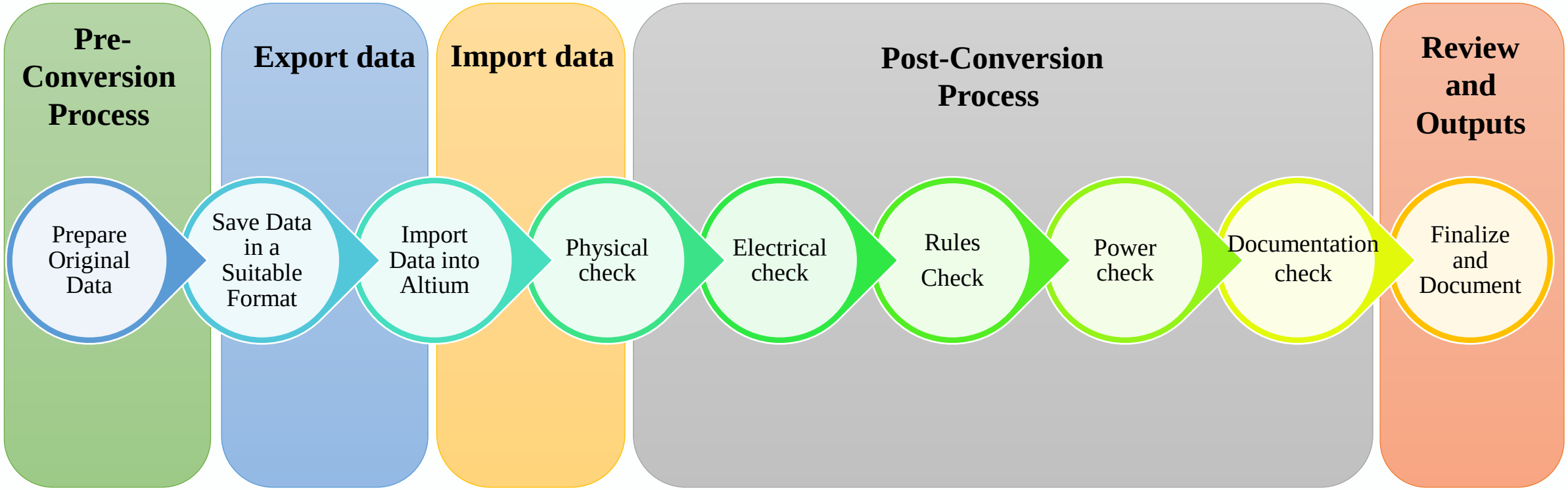
Advanced borescopes are essential tools across various industries, facilitating thorough internal inspections without the necessity of extensive disassembly. Their capability to capture high-resolution images and videos allows professionals to identify problems early, thereby ensuring safety, enhancing efficiency, and maintaining quality control in operations.

Challenges – EDA Conversion

The client approached us with the task of converting their schematics and PCB files from **PADS** to **Altium Designer** to effectively meet their requirements.

- To Achieve 99.99% Physical Accuracy
- To Achieve 100% Electrical Match
- Manage Length Matching Groups
- Accurate Footprint Libraries
- Netlist Synchronization
- Design Rule Translation
- Handling Custom Components

EDA Conversion - SoW



Pre-Conversion Process

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Prepare original data

- Check content
- Remove redundant or confusing data
- Verify integrity

Library Considerations

- Ensure that schematic symbols match the correct PCB footprints.
- Verify supply chain data and Bill of Materials (BoM) parameters for accuracy.
- Import 3D component information where required for visual representation.
- Confirm that custom pads, copper shapes, solder mask, and resist layers are properly defined.

Schematic Considerations

- Ensure proper representation of power objects with single-pin components.
- Avoid ambiguous connectivity and hidden pins.
- Maintain consistent local net names and case sensitivity.
- Ensure the schematic aligns with the PCB design.

PCB Considerations

- Limit excessive graphical objects on documentation layers.
- Properly define star point earths and address DRC violations.
- Confirm PCB boundaries and layer assignments.
- Match auto-named nets with the schematic.

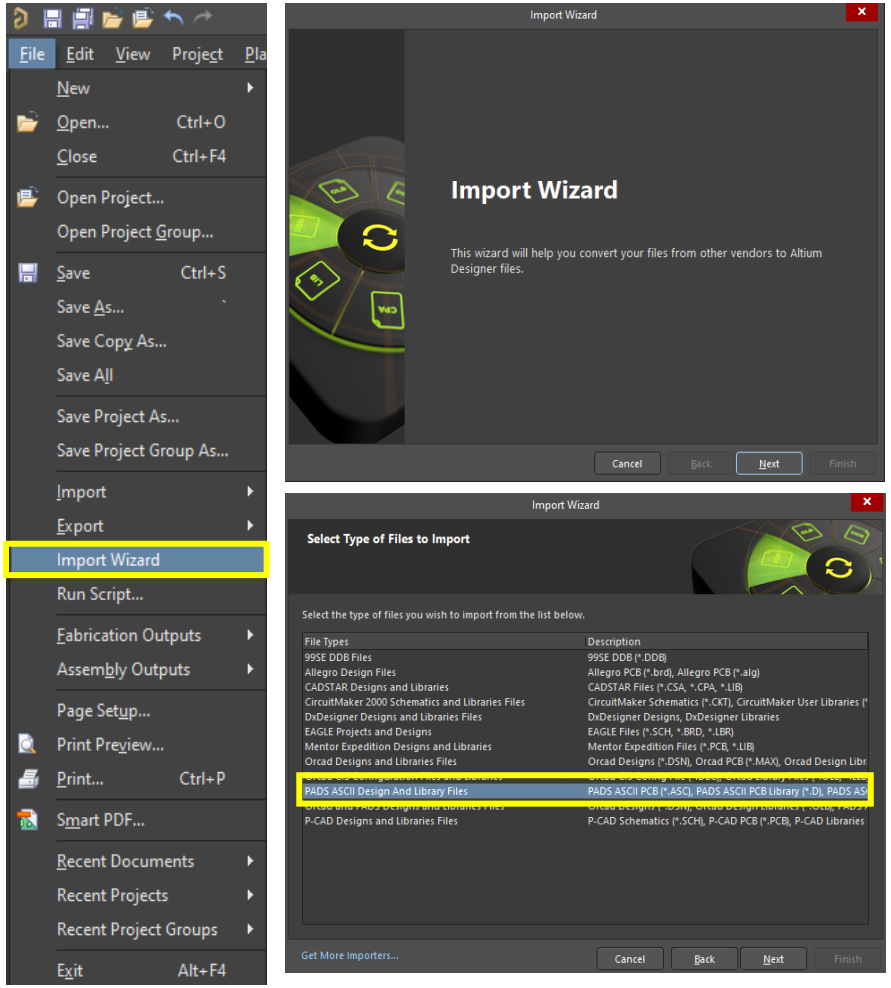
Export Data From PADS

Save and export data from PADS in a suitable format to import into Altium Designer.

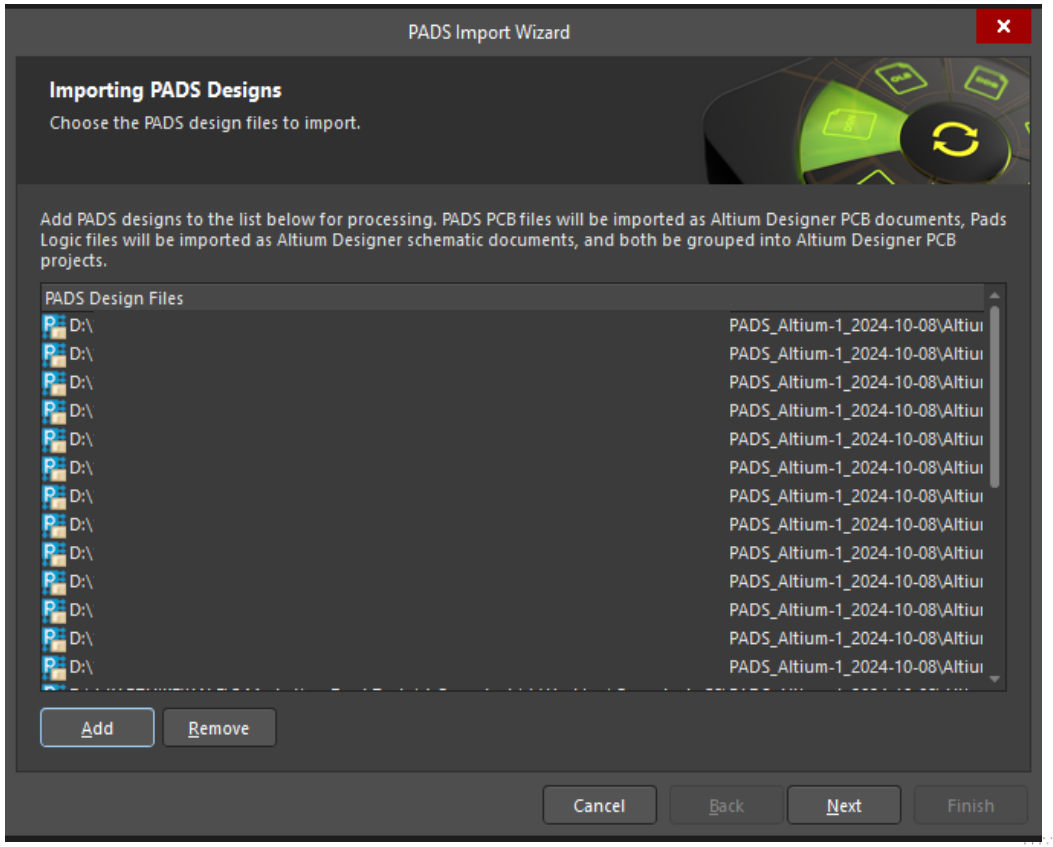
	PADS	Altium
PCB Layout	(*.ASC) ASCII PCB files	(*.PcbDoc).
Schematics	(*.TXT) ASCII Schematic files	(*.SchDoc).
Schematic library	(*.c)	(*.SchLib).
PCB library	(*.d)	(*.PcbLib).

- Translated PADS schematics and PCB files are not automatically grouped into one PCB project, a project is created for the schematics and another for the PCB.

Import Data into Altium



Importing PADS Files



Import Data into Altium

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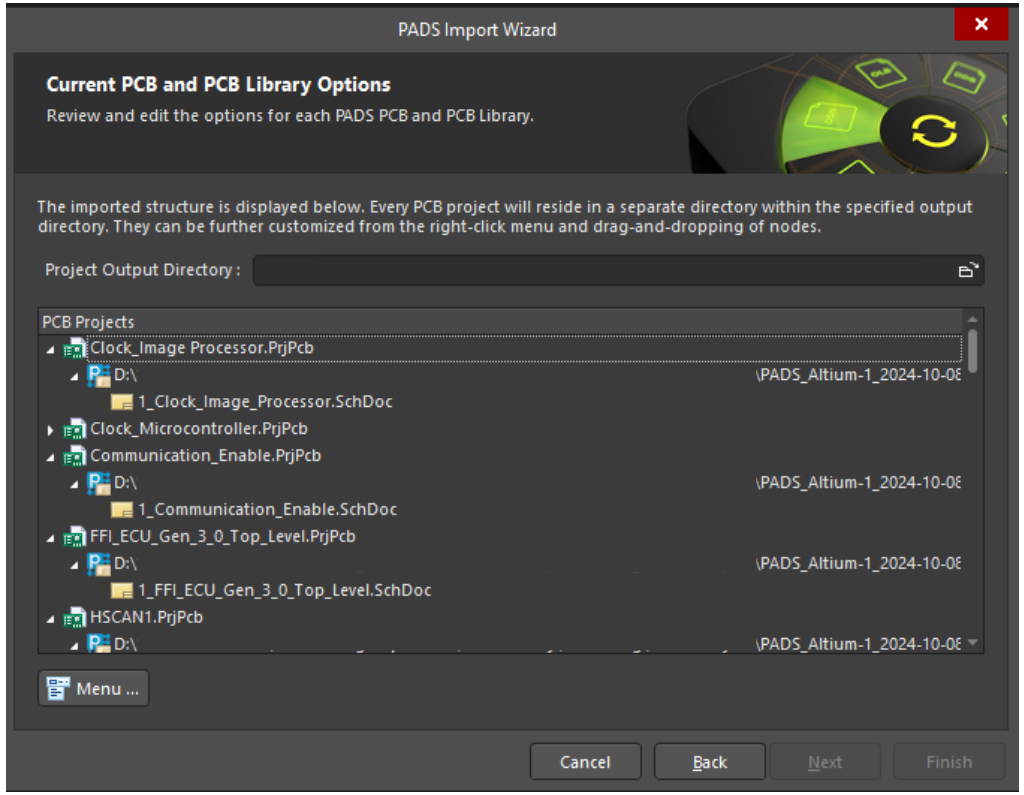
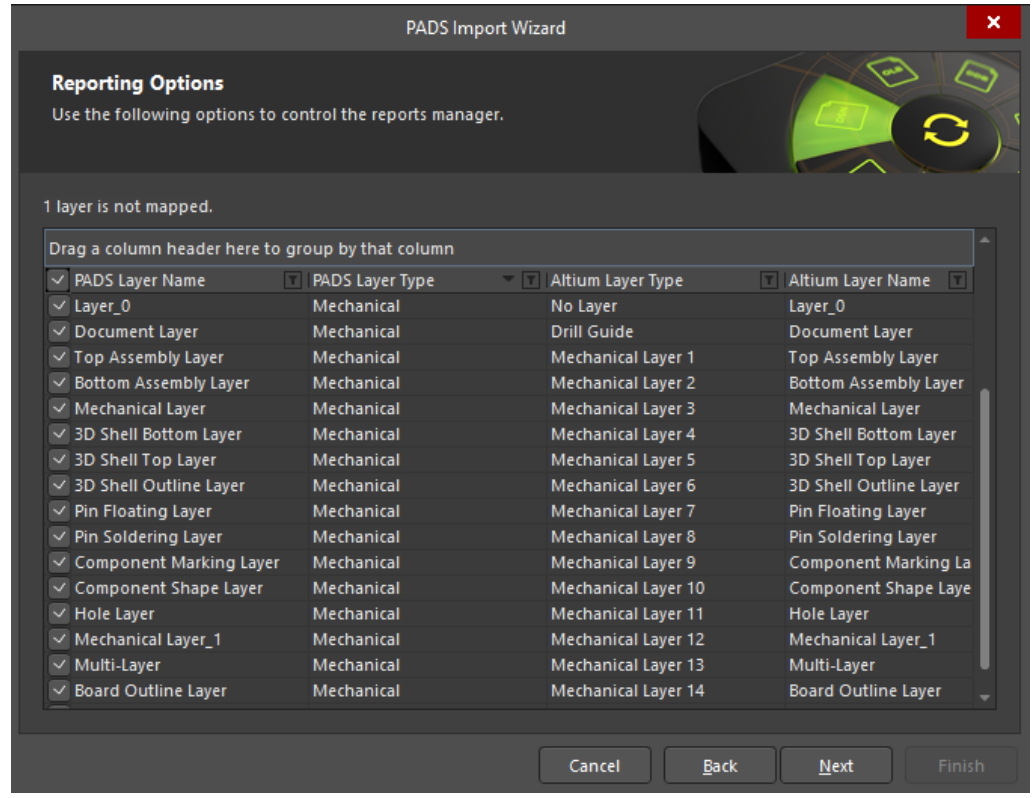
Convert as Altium Files



Layer Mapping



Import Data into Altium

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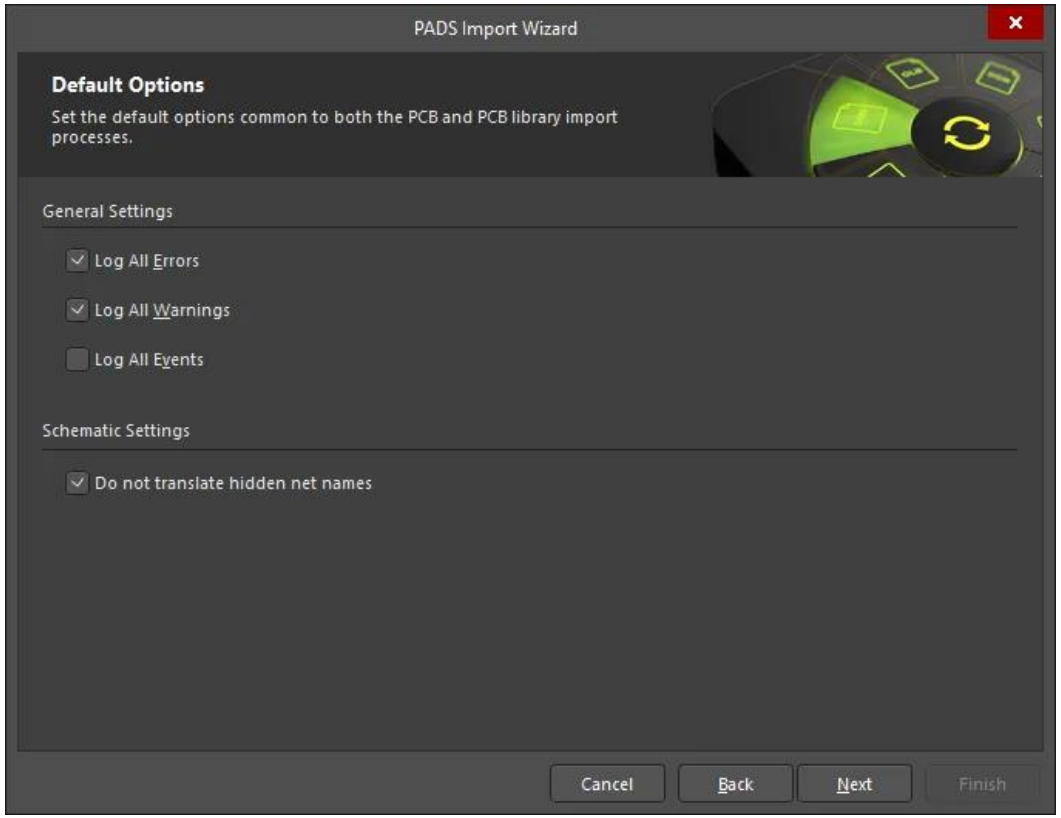
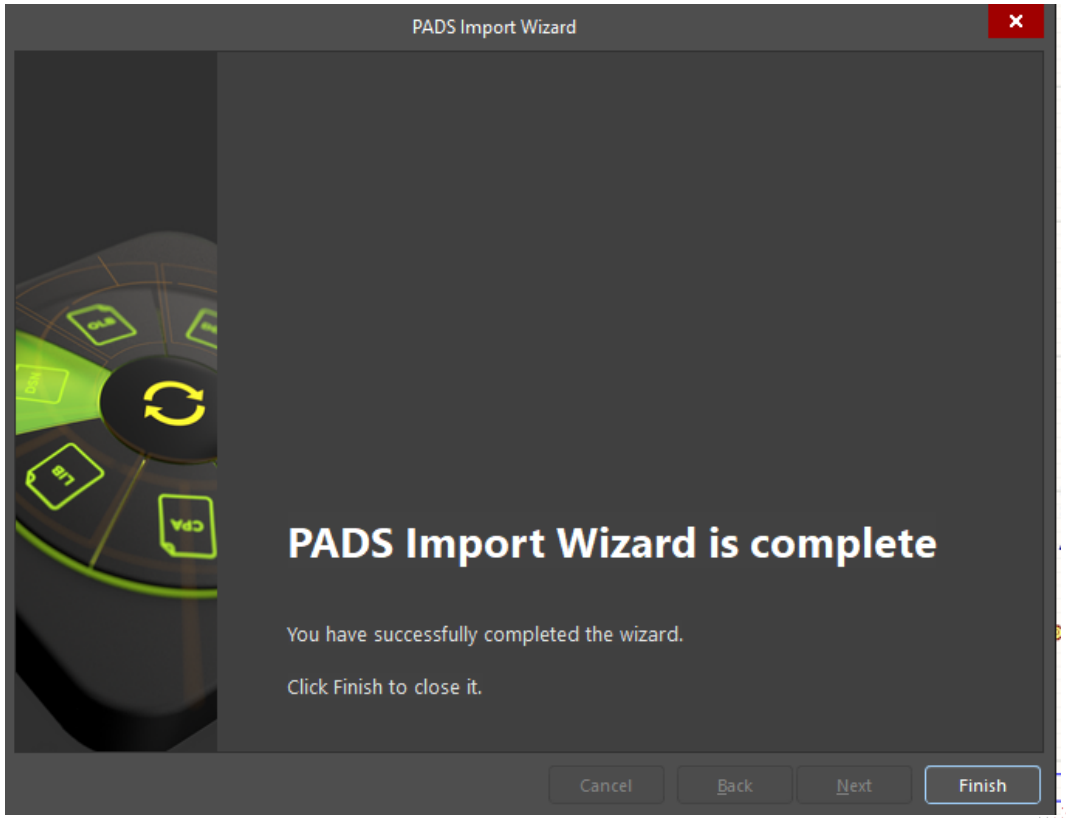
NetNames options

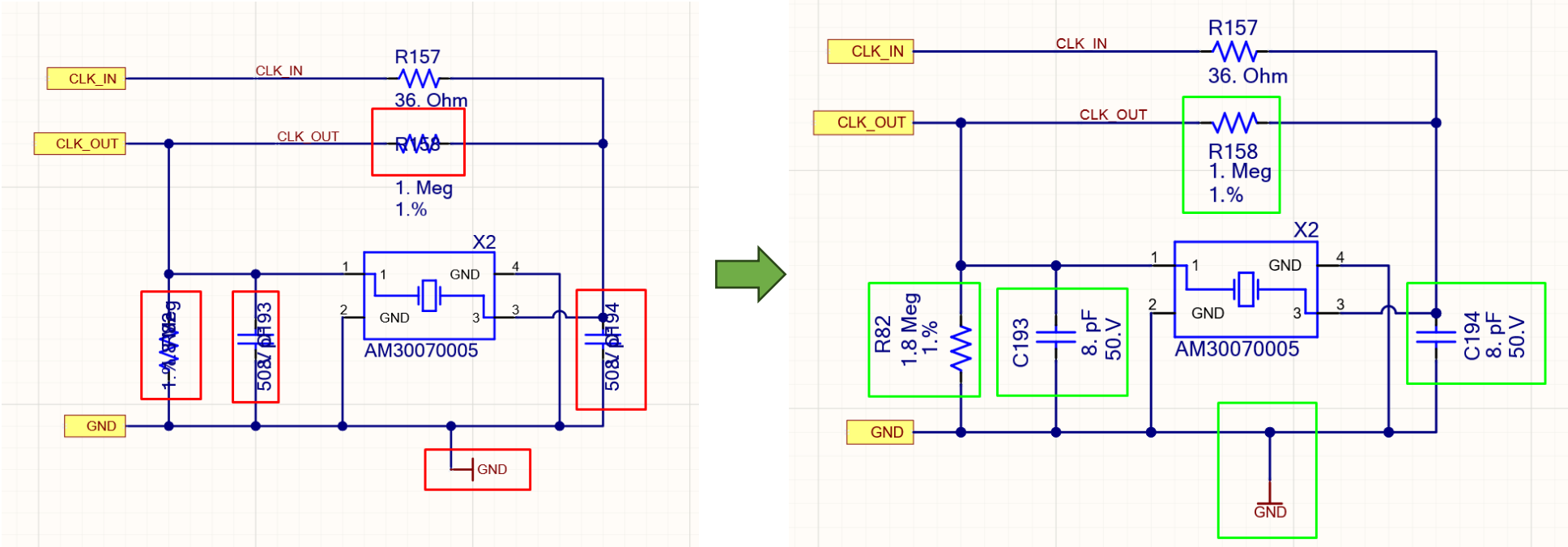


Import Completed



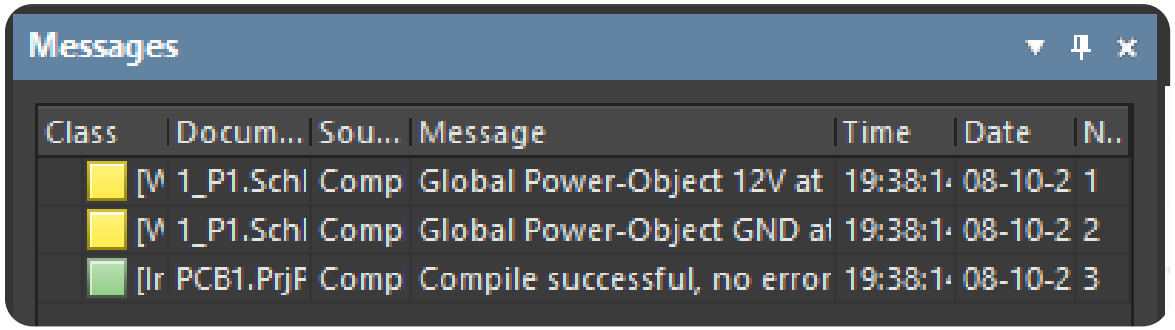
Schematic Check

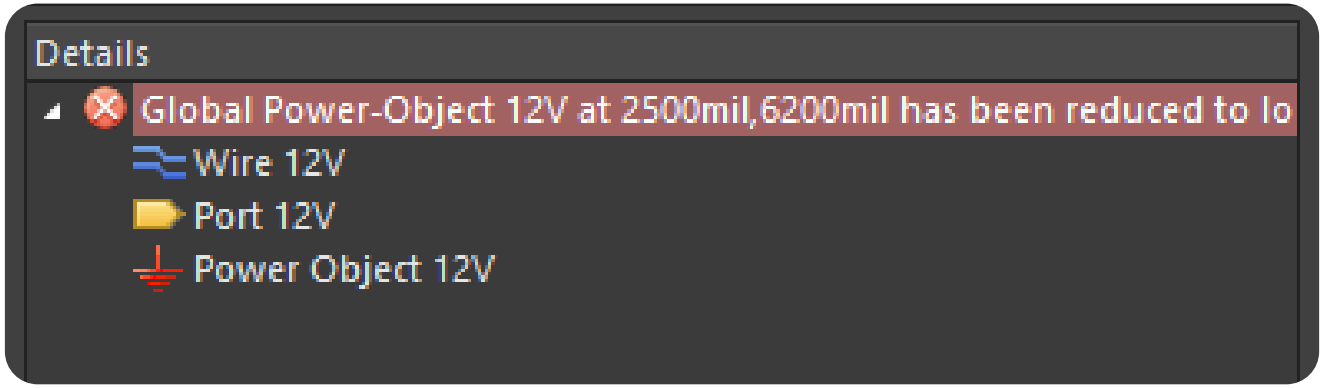
- Performed a visual check of the imported schematic and confirm that the location of each Net Label is appropriate.
- Go over the schematic visually, ensuring readability from a design perspective. If something is unclear at a glance, adjust it.



Schematic Validation

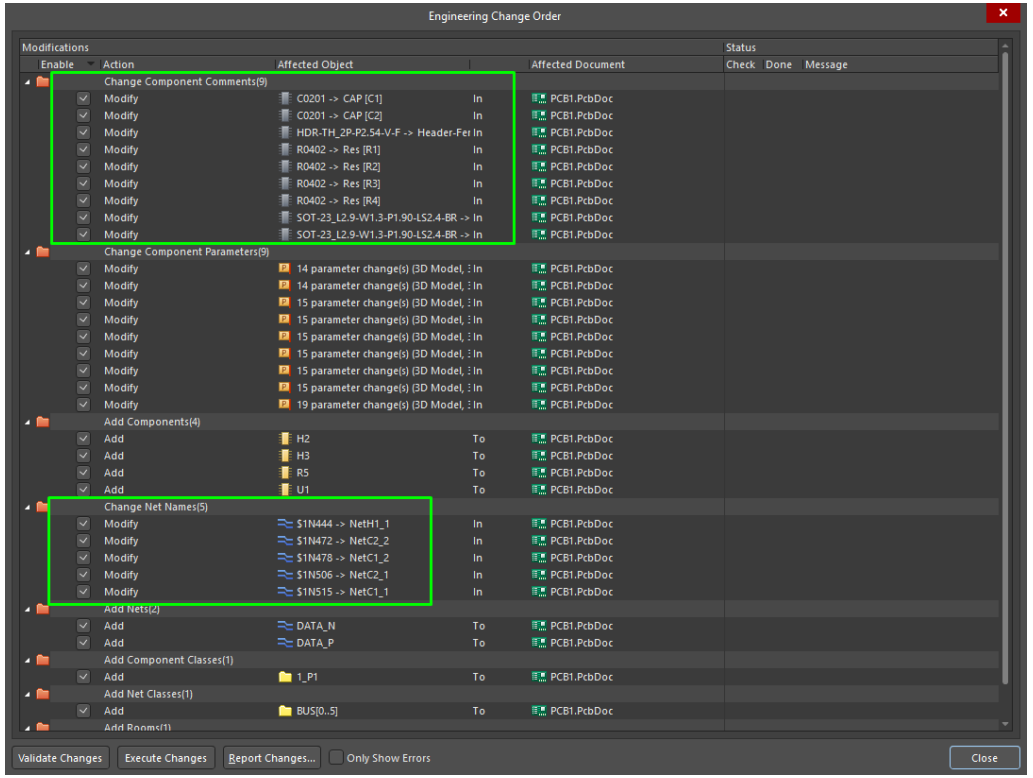
- Before synchronizing the schematic with the PCB, the schematic was validated to ensure there were no connectivity issues.
- The Project » Validate PCB Project <ProjectName> command was executed, and the validation results were displayed in the Messages panel.





Schematic to PCB Synchronization

- After matching schematic components to PCB equivalents, one schematic sheet was set as active in Altium Designer.
- The **Design » Update PCB Document <PcbName>** command was then used to open the **Engineering Change Order (ECO)** dialog box, which displayed the necessary PCB changes.
- Changes did not need to be applied all at once; specific ECOs were managed using checkboxes or the right-click context menu to disable unwanted changes.
- The ECO dialog buttons **validated and executed** the enabled changes, and the dialog was closed by clicking the Close button.



Verifying the PCB Design

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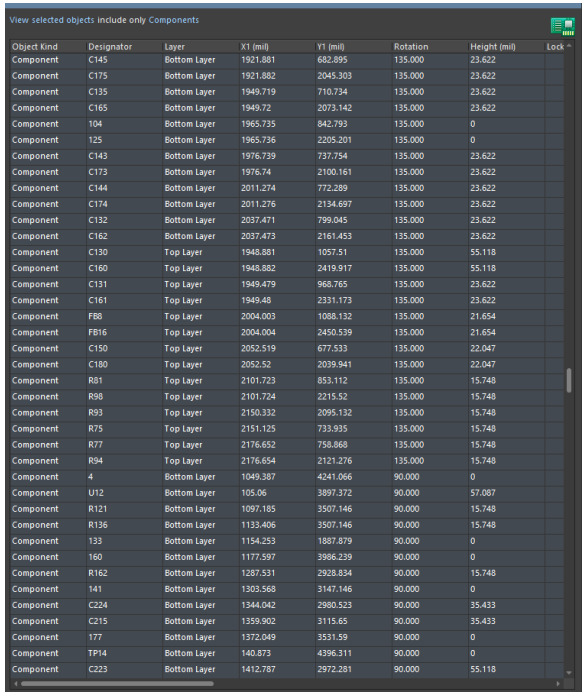
- Check that the physical layout in Altium Designer matches the original design from PADS.
- This includes verifying the accuracy of layer mapping and confirming that all components are placed correctly according to the original design specifications.

Components location's Verification

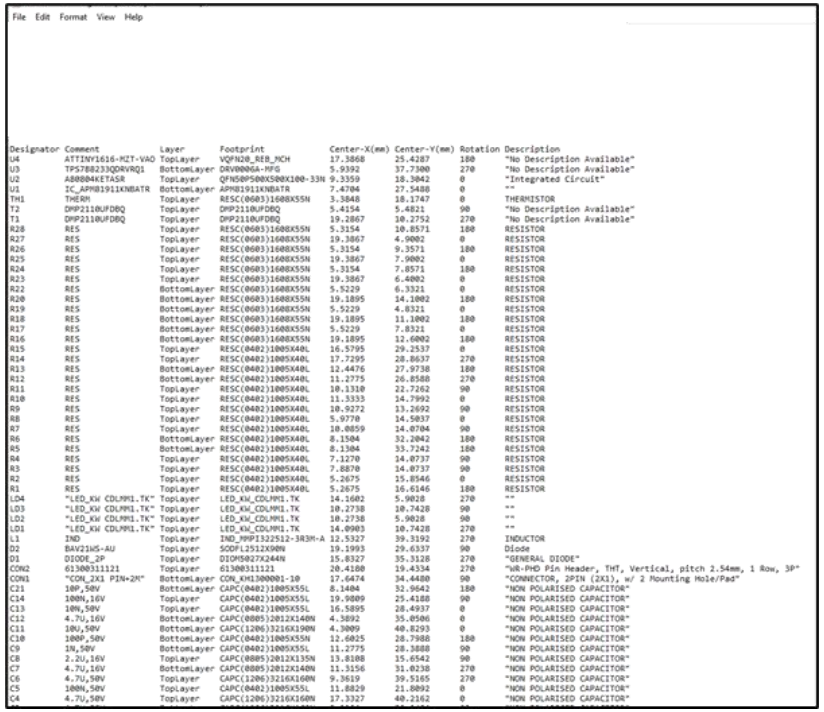
Altium PCB Details



Object Kind	Designator	Layer	X1 (mil)	Y1 (mil)	Rotation	Height (mil)
Component	C145	Bottom Layer	1921.881	682.895	135.000	23.622
Component	C175	Bottom Layer	1921.882	2045.303	135.000	23.622
Component	C135	Bottom Layer	1949.719	710.734	135.000	23.622
Component	C165	Bottom Layer	1949.72	2073.142	135.000	23.622
Component	104	Bottom Layer	1965.735	842.793	135.000	0
Component	125	Bottom Layer	1965.736	2205.201	135.000	0
Component	C143	Bottom Layer	1976.739	737.754	135.000	23.622
Component	C173	Bottom Layer	1976.74	2100.161	135.000	23.622
Component	C144	Bottom Layer	2011.274	772.289	135.000	23.622
Component	C174	Bottom Layer	2011.276	2134.697	135.000	23.622
Component	C132	Bottom Layer	2037.471	799.045	135.000	23.622
Component	C162	Bottom Layer	2037.473	2161.453	135.000	23.622
Component	C130	Top Layer	1948.881	1057.51	135.000	55.118
Component	C160	Top Layer	1948.882	2419.917	135.000	55.118
Component	C131	Top Layer	1949.479	968.765	135.000	23.622
Component	C161	Top Layer	1949.48	2331.173	135.000	23.622
Component	FB8	Top Layer	2004.003	1088.132	135.000	21.654
Component	FB16	Top Layer	2004.004	2450.539	135.000	21.654
Component	C150	Top Layer	2052.519	677.533	135.000	22.047
Component	C180	Top Layer	2052.52	2039.941	135.000	22.047
Component	R81	Top Layer	2101.723	853.112	135.000	15.748
Component	R98	Top Layer	2101.724	2215.52	135.000	15.748
Component	R93	Top Layer	2150.332	2095.132	135.000	15.748
Component	R75	Top Layer	2151.125	733.935	135.000	15.748
Component	R77	Top Layer	2176.652	758.868	135.000	15.748
Component	R94	Top Layer	2176.654	2121.276	135.000	15.748
Component	4	Bottom Layer	1049.387	4241.066	90.000	0
Component	U12	Bottom Layer	105.06	3897.372	90.000	57.087
Component	R121	Bottom Layer	1097.185	3507.146	90.000	15.748
Component	R136	Bottom Layer	1133.406	3507.146	90.000	15.748
Component	133	Bottom Layer	1154.253	1887.879	90.000	0
Component	160	Bottom Layer	1177.597	3986.239	90.000	0
Component	R162	Bottom Layer	1287.531	2928.834	90.000	15.748
Component	141	Bottom Layer	1303.568	3147.146	90.000	0
Component	C224	Bottom Layer	1344.042	2980.523	90.000	35.433
Component	C215	Bottom Layer	1359.902	3115.65	90.000	35.433
Component	177	Bottom Layer	1372.049	3531.59	90.000	0
Component	TP14	Bottom Layer	140.873	4396.311	90.000	0
Component	C223	Bottom Layer	1412.787	2972.281	90.000	55.118

Compare

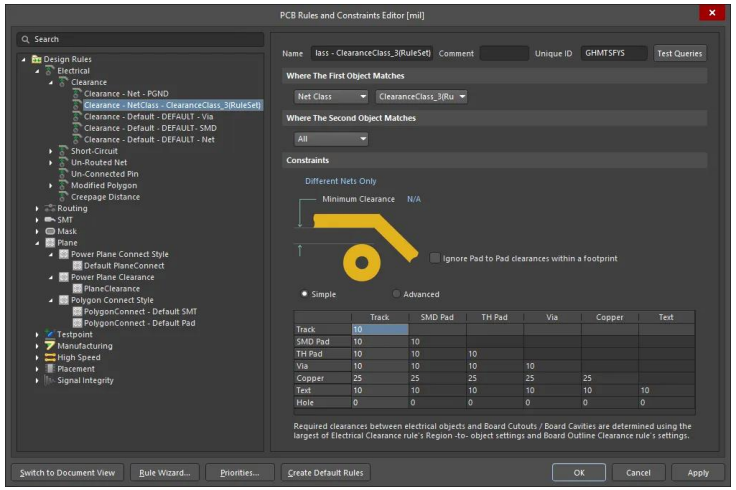
PADS PCB Details



Designator	Comment	Layer	Footprint	Center-X(mm)	Center-Y(mm)	Rotation	Description
U4	ATTINY1616-MZT-VAO	TopLayer	VQFN20_REB_MCH	17.3868	25.4287	180	"No Description Available"
U3	TPS78233QDRVRQ1	BottomLayer	DRV0006A-MFG	5.9392	37.7300	270	"No Description Available"
U2	AB0004KETASR	TopLayer	QFN50P500X500X100-33N	9.3359	18.3042	0	"Integrated Circuit"
U1	IC_APH8191XNBATR	BottomLayer	APH8191XNBATR	7.4704	27.5488	0	""
TH1	THERM	TopLayer	RESC(0603)1608X55N	3.3848	18.1747	0	THERMISTOR
T2	DMP2110UFDBQ	TopLayer	DMP2110UFDBQ	5.4154	5.4821	90	"No Description Available"
T1	DMP2110UFDBQ	TopLayer	DMP2110UFDBQ	19.2867	10.2752	270	"No Description Available"
R28	RES	TopLayer	RESC(0603)1608X55N	5.3154	10.8571	180	RESISTOR
R27	RES	TopLayer	RESC(0603)1608X55N	19.3867	4.9002	0	RESISTOR
R26	RES	TopLayer	RESC(0603)1608X55N	5.3154	9.3571	180	RESISTOR
R25	RES	TopLayer	RESC(0603)1608X55N	19.3867	7.9002	0	RESISTOR
R24	RES	TopLayer	RESC(0603)1608X55N	5.3154	7.8571	180	RESISTOR
R23	RES	TopLayer	RESC(0603)1608X55N	19.3867	6.4002	0	RESISTOR
R22	RES	BottomLayer	RESC(0603)1608X55N	5.5229	6.3321	0	RESISTOR
R20	RES	BottomLayer	RESC(0603)1608X55N	19.1895	14.1002	180	RESISTOR
R19	RES	BottomLayer	RESC(0603)1608X55N	5.5229	4.8321	0	RESISTOR
R18	RES	BottomLayer	RESC(0603)1608X55N	19.1895	11.1002	180	RESISTOR
R17	RES	BottomLayer	RESC(0603)1608X55N	5.5229	7.8321	0	RESISTOR
R16	RES	BottomLayer	RESC(0603)1608X55N	19.1895	12.6002	180	RESISTOR
R15	RES	TopLayer	RESC(0402)1005X40L	16.5795	29.2537	0	RESISTOR
R14	RES	TopLayer	RESC(0402)1005X40L	17.7295	28.8637	270	RESISTOR
R13	RES	BottomLayer	RESC(0402)1005X40L	12.4476	27.9738	180	RESISTOR
R12	RES	BottomLayer	RESC(0402)1005X40L	11.2775	26.8588	270	RESISTOR
R11	RES	TopLayer	RESC(0402)1005X40L	10.1310	22.7262	90	RESISTOR
R10	RES	TopLayer	RESC(0402)1005X40L	11.3333	14.7992	0	RESISTOR
R9	RES	TopLayer	RESC(0402)1005X40L	10.9272	13.2692	90	RESISTOR
R8	RES	TopLayer	RESC(0402)1005X40L	5.9770	14.5037	0	RESISTOR
R7	RES	TopLayer	RESC(0402)1005X40L	10.0859	14.0704	90	RESISTOR
R6	RES	BottomLayer	RESC(0402)1005X40L	8.1504	32.2042	180	RESISTOR
R5	RES	BottomLayer	RESC(0402)1005X40L	8.1304	33.7242	180	RESISTOR
R4	RES	TopLayer	RESC(0402)1005X40L	7.1270	14.0737	90	RESISTOR
R3	RES	TopLayer	RESC(0402)1005X40L	7.8870	14.0737	90	RESISTOR
R2	RES	TopLayer	RESC(0402)1005X40L	5.2675	15.8546	0	RESISTOR
R1	RES	TopLayer	RESC(0402)1005X40L	5.2675	16.6146	180	RESISTOR
LD4	"LED_KW CDLMM1.TK"	TopLayer	LED_KW_CDLMM1.TK	14.1602	5.9028	270	""
LD3	"LED_KW CDLMM1.TK"	TopLayer	LED_KW_CDLMM1.TK	10.2738	10.7428	90	""
LD2	"LED_KW CDLMM1.TK"	TopLayer	LED_KW_CDLMM1.TK	10.2738	5.9028	90	""
LD1	"LED_KW CDLMM1.TK"	TopLayer	LED_KW_CDLMM1.TK	14.0903	10.7428	270	""
L1	IND	TopLayer	IND_MPP1322512-3R3M-A	12.5327	39.3192	270	INDUCTOR
D2	BAV21WS-AU	TopLayer	SODFL2512X98N	19.1993	29.6337	90	Diode
D1	DIODE_2P	TopLayer	DIOM5027X244N	15.8327	35.3128	270	"GENERAL DIODE"
CON2	61300311121	TopLayer	61300311121	20.4180	19.4334	270	"WR-PHD Pin Header, THT, Vertical, pitch 2.54mm, 1 Row, 3P"
CON1	"CON_2X1 PIN+2M"	BottomLayer	CON_KH1300001-10	17.6474	34.4480	90	"CONNECTOR, 2PIN (2X1), w/ 2 Mounting Hole/Pad"
C21	100P,50V	BottomLayer	CAPC(0402)1005X55L	8.1404	32.9642	180	"NON POLARISED CAPACITOR"
C14	100N,16V	TopLayer	CAPC(0402)1005X55L	19.9809	25.4188	90	"NON POLARISED CAPACITOR"
C13	10N,50V	TopLayer	CAPC(0402)1005X55L	16.5895	28.4937	0	"NON POLARISED CAPACITOR"
C12	4.7U,16V	BottomLayer	CAPC(0805)2012X140N	4.3892	35.0506	0	"NON POLARISED CAPACITOR"
C11	10U,50V	BottomLayer	CAPC(1206)3216X190N	4.3009	40.8293	0	"NON POLARISED CAPACITOR"
C10	100P,50V	BottomLayer	CAPC(0402)1005X55N	12.6025	28.7988	180	"NON POLARISED CAPACITOR"
C9	1N,50V	BottomLayer	CAPC(0402)1005X55L	11.2775	28.3888	90	"NON POLARISED CAPACITOR"
C8	2.2U,16V	TopLayer	CAPC(0805)2012X135N	13.8108	15.6542	90	"NON POLARISED CAPACITOR"
C7	4.7U,16V	BottomLayer	CAPC(0805)2012X140N	11.3156	31.0238	270	"NON POLARISED CAPACITOR"
C6	4.7U,50V	TopLayer	CAPC(1206)3216X160N	9.3619	39.5165	270	"NON POLARISED CAPACITOR"
C5	100N,50V	TopLayer	CAPC(0402)1005X55L	11.8829	21.8092	0	"NON POLARISED CAPACITOR"
C4	4.7U,50V	TopLayer	CAPC(1206)3216X160N	17.3327	40.2162	0	"NON POLARISED CAPACITOR"

Verifying the PCB Design

Review the Design Rules



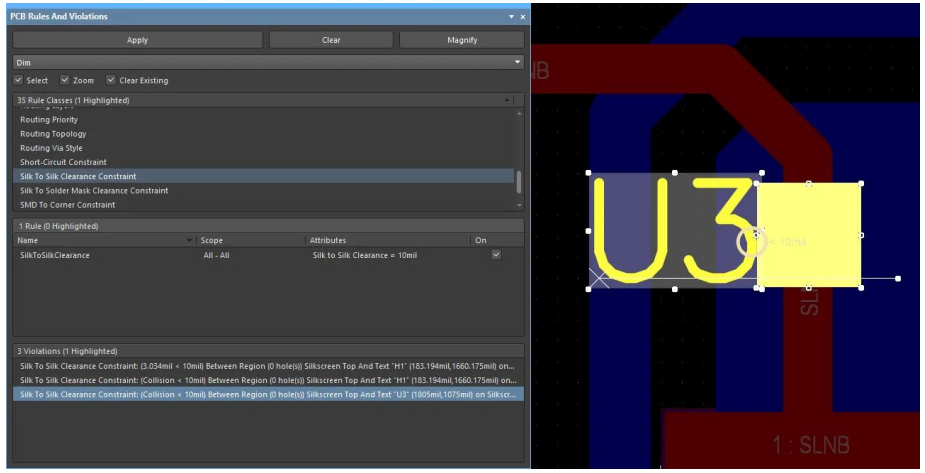
- The **Design Rules** were reviewed **(Design » Rules)**, focusing on the Electrical Clearance, Plane Connect, and Clearance rules.

- In Altium Designer, the rules existed independently of the objects, with applicable object(s) defined by their rule scope in the "Where the Object Matches" section of each rule.

Perform a Design Rule Check

- The DRC check was successfully implemented to identify design rule violations.

- All identified errors were promptly rectified.
  (Both Electrical (Cu Layers) and Non electrical layers (Overlay, Assembly, etc.) are also verified and cleaned up.)



Ensure Electrical Accuracy

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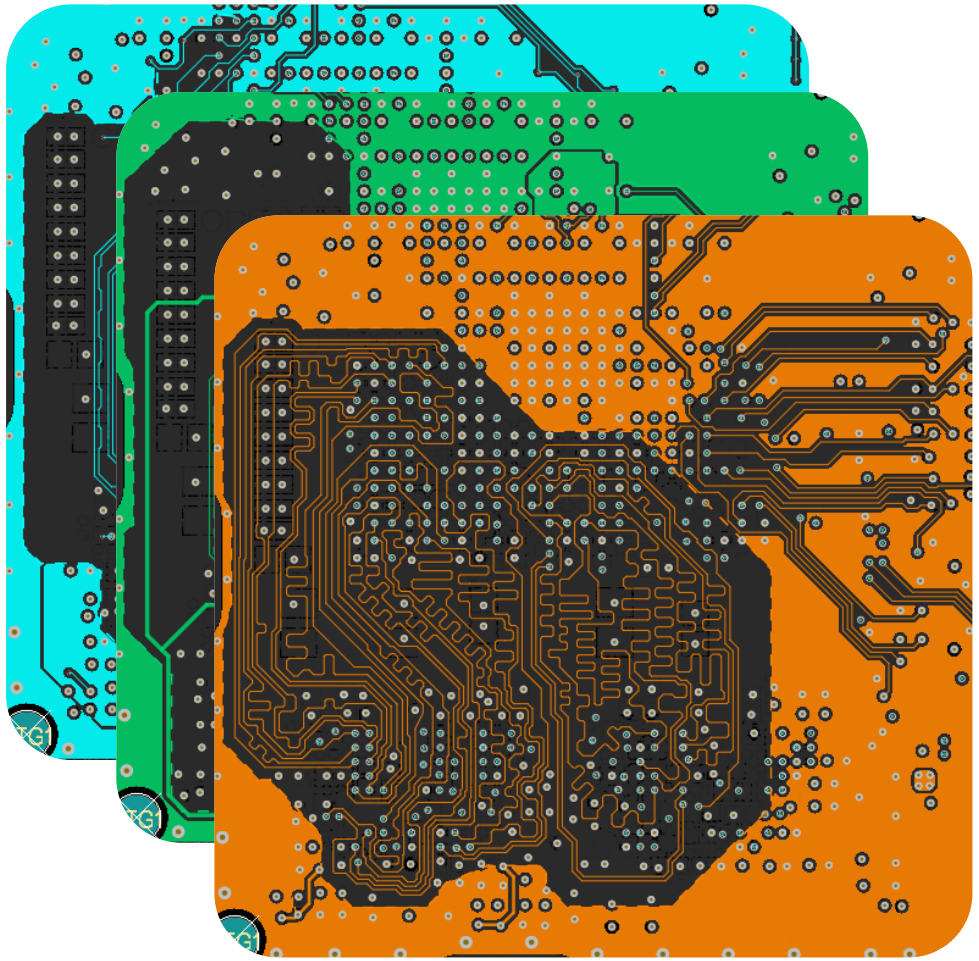
- The netlists from PADS were synchronized with those in Altium Designer to maintain electrical connectivity and signal integrity.
- This ensured that high-speed signals and critical electrical connections were accurately represented, preventing potential performance issues.

Routing	
Routing Information	
Routing completion	100.00%
Connections	1872
Connections routed	1872
Connections remaining	0

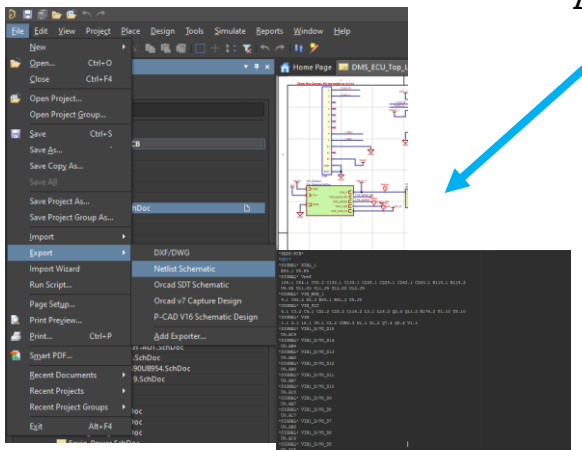


Signals routing Verification

Netlist Verification

- A netlist was generated in Altium Designer and subsequently compared with the netlist from PADS for verification.

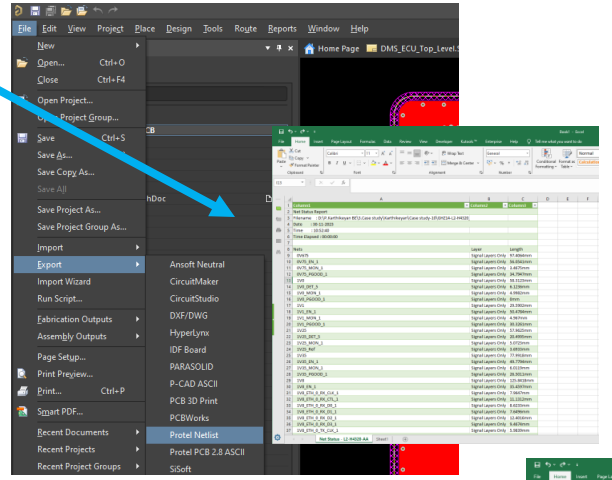
Schematic Netlist



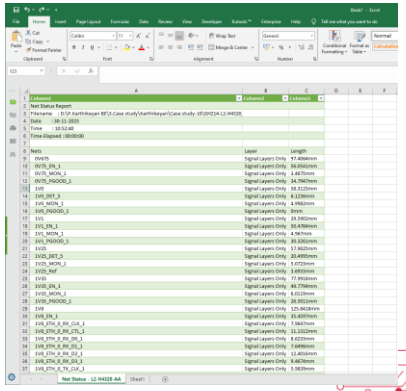
Altium Netlist

Compare

PCB Netlist



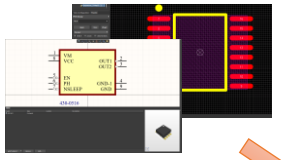
Compare



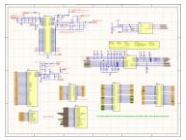
PADS Netlist

Finalize and Document

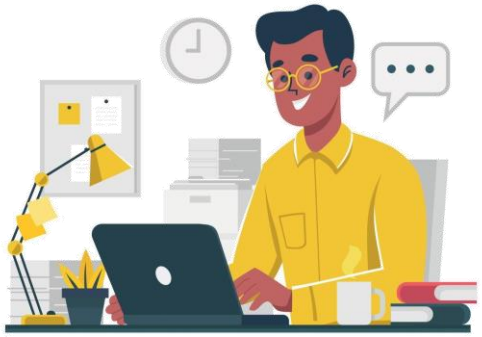
- The PCB design documentation, including schematics, layout files, and design notes, was updated.
- The final design files were saved and backed up properly, providing a complete record of the converted design.



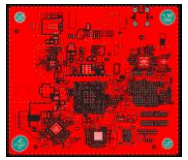
Library Files



Schematics



Final Review



PCB layout files

Results-In Altium Designer

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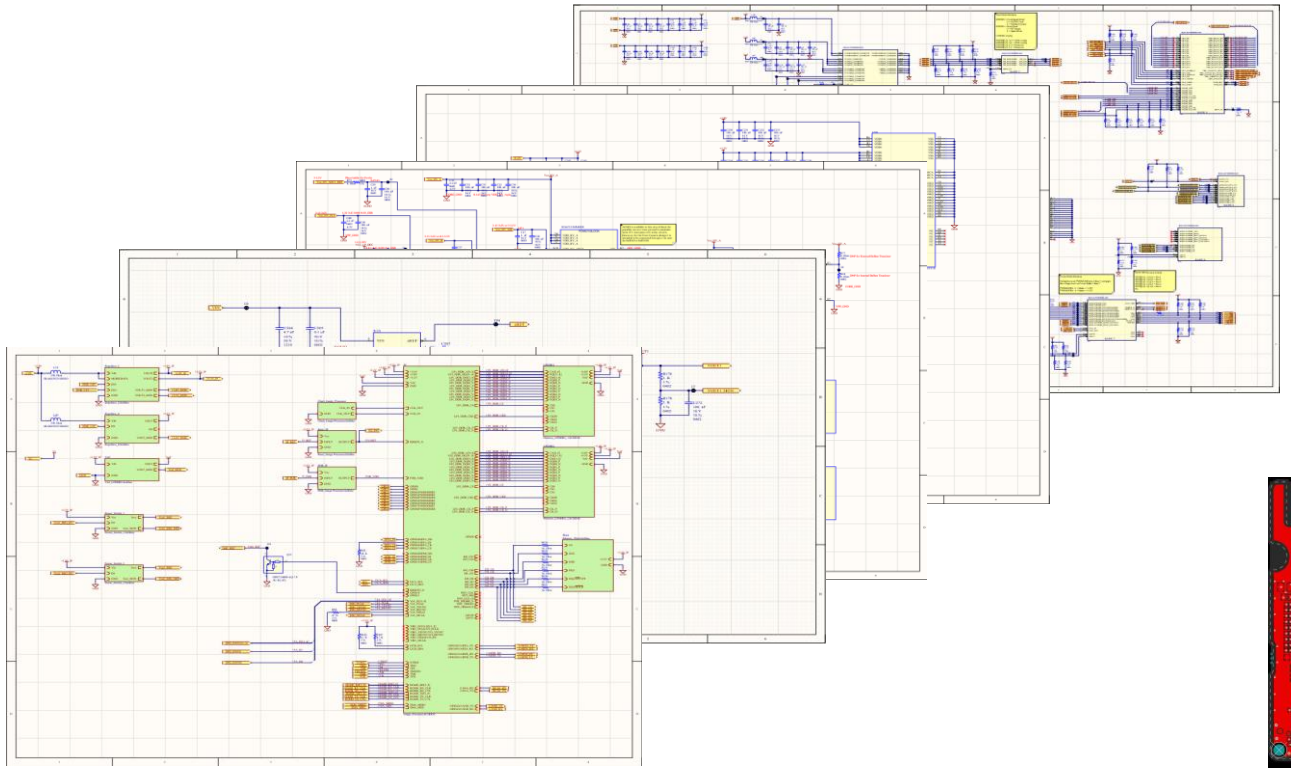
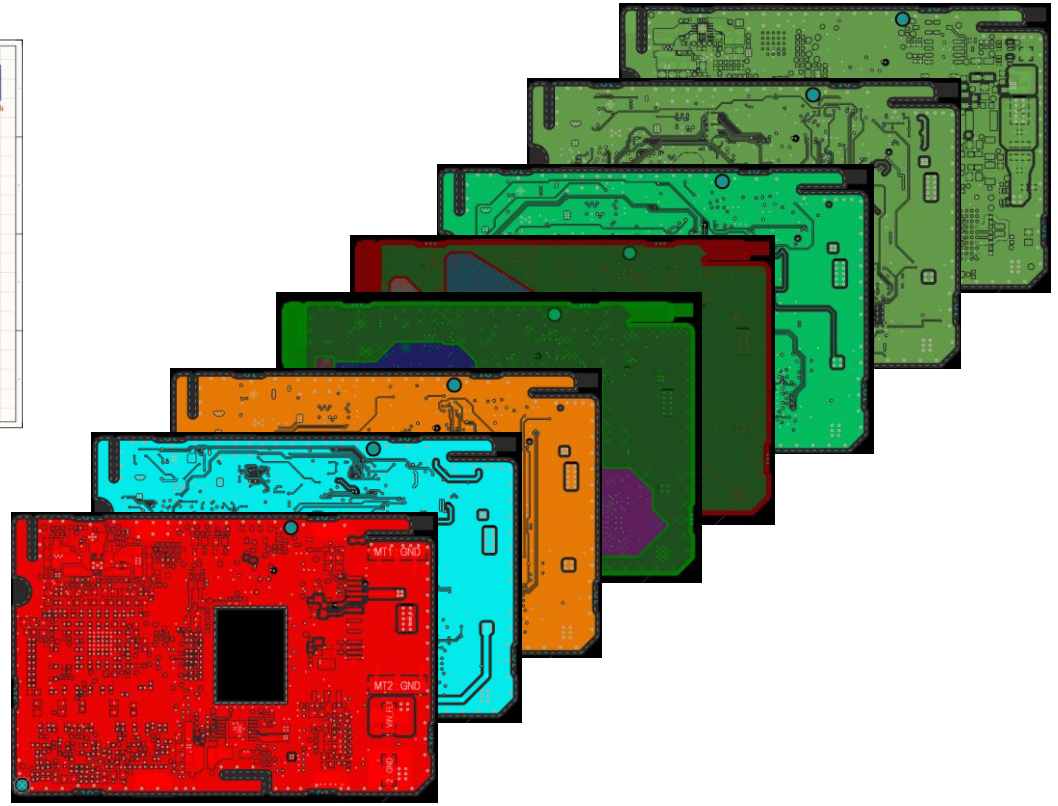
Schematics



PCB Layout



"The EDA conversion from PADS PCB to Altium Designer ensured complete electrical accuracy and an outstanding 99.99% physical precision."

GigHz
A Global Engineering partner

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Client Testimonial

Here's a testimonial from a satisfied client that showcases the effectiveness of our EDA conversion services,

"Working with GigHz was a transformative experience for us. Their expert conversion of our PCB design files from PADS to Altium Designer was defined by remarkable efficiency, precision, and dedication. They consistently met our deadlines and delivered cost-effective solutions that aligned perfectly with our expectations. The quality of their work, marked by exceptional attention to detail and flawless execution, surpassed all our requirements. GigHz exemplifies the ideal combination of time efficiency, cost-effectiveness, and unmatched quality, making them an invaluable partner in navigating the complexities of electronic design and PCB development."

Conclusion

We showcased our dedication to quality by delivering EDA conversion results that perfectly met the client's requirements.

Our collaboration blends deep technical knowledge with personalized service, highlighting our proficiency and focus on client satisfaction.

We provide high-quality EDA conversion PCB layouts that reduce costs while demonstrating our capability and reliability.

Our approach emphasizes quality and strict adherence to deadlines, ensuring consistent and exceptional performance.