



Efficient PCB Layout for DMS Systems

Scope: Complete End-to-End PCB Layout Design

Application: Advanced Driver Assistance Systems (ADAS)

Driver Monitoring Systems (DMS) are vital for the safety and efficiency of Advanced Driver Assistance Systems (ADAS). The performance and reliability of these systems depend significantly on the quality of the PCB (Printed Circuit Board) layout. A thorough and well-executed end-to-end PCB layout design is crucial for ensuring that the DMS operates effectively and reliably.

This Case study focuses on the complete end-to-end PCB layout design process and its impact on enhancing the reliability of DMS within ADAS applications. We will examine how optimizing each stage of the PCB design—from initial planning and component placement to final routing—can improve system performance, reduce errors, and ensure robust operation.



Challenges

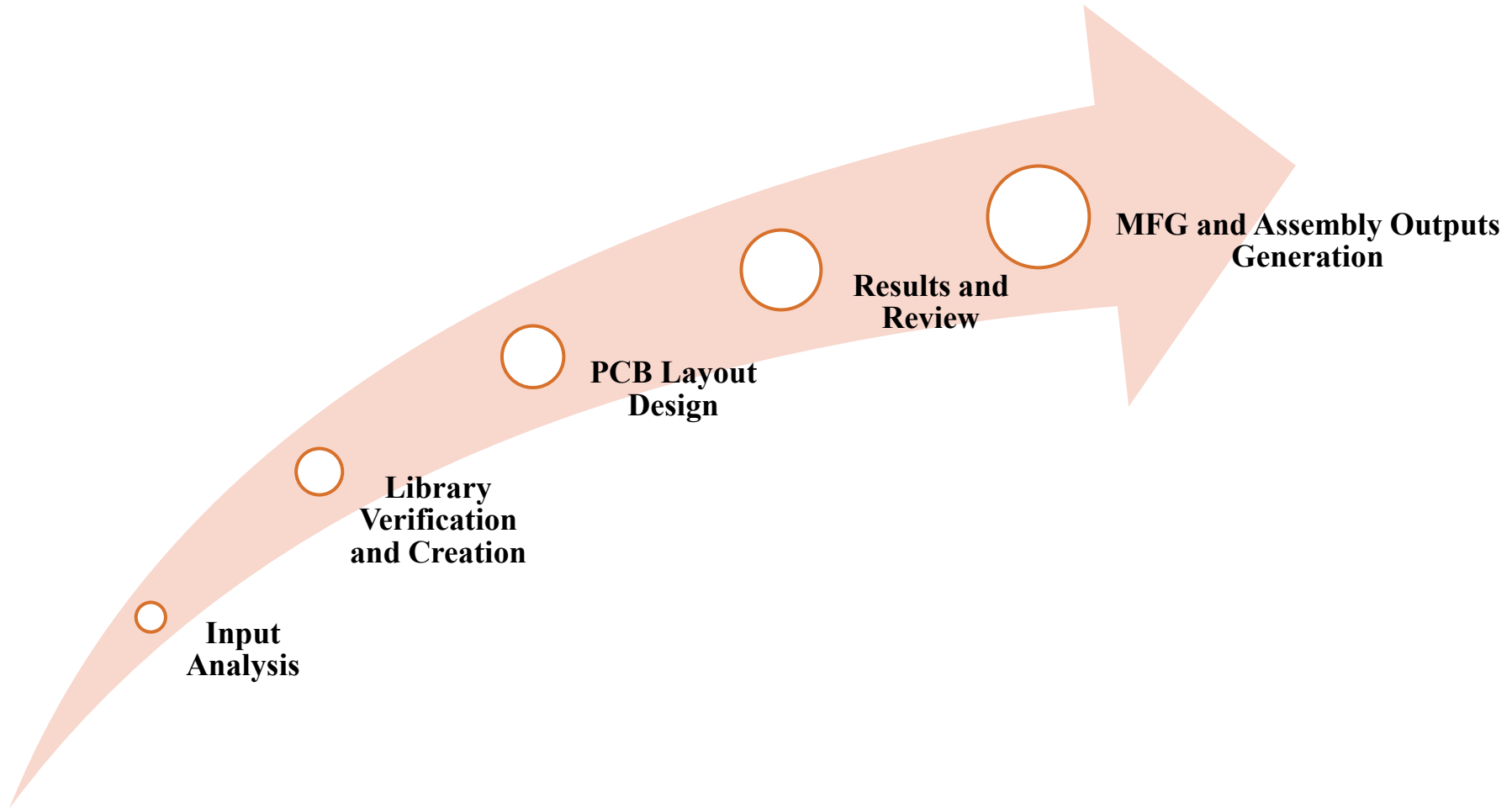
The client has tasked us with updating their existing PCB version, which involves a complete redesign of the PCB layout, including schematic verification to generating manufacturing outputs.

Challenges:

- Check and update the library to meet standards, especially for non-standard components.
- Build a library for project-specific components not currently in the database.
- Increased component count and a reduced board size.
- Maintain critical component sections from the previous version to preserve signal integrity without altering their locations.
- Design effective power distribution and Ensure compliance with EMI/EMC standards.
- Incorporate Design for Manufacturing (DFM) considerations.
- Address requirements for multiple high-speed signal groups.



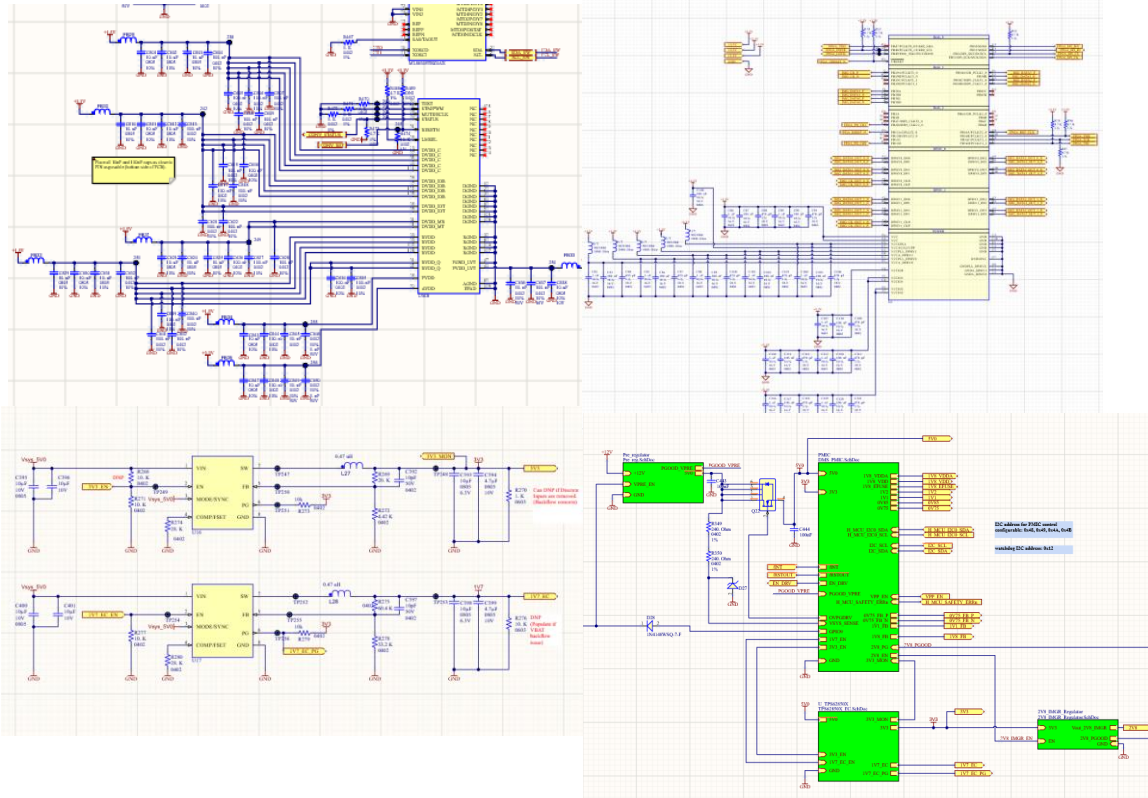
PCB Layout Design - SoW



Input Analysis

PCB Project contains,

- Total components → 2089
- Layer count → 12
- Total connection → 4512
- Dimension → 220mm X 53mm
- Pin count → 4440
- No. of powers → 16
- No. of High speed signal Groups → 10
- Devices → Video processor (TFBGA196), LPDDR4, Microprocessor (FCBGA-484), Deserializer, Microcontroller, Display controller, PMICs, Buck and Boos converters
- BGA Pitch
- 0.8mm X 0.8 mm - MPSoC
- 0.8mm X 0.65mm - DDR4
- 0.65mm X 0.65mm - Video Processor

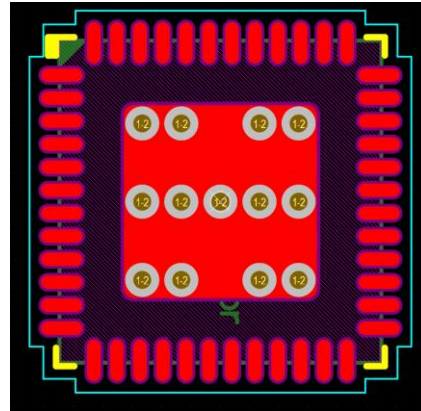


Library Verification and Creation

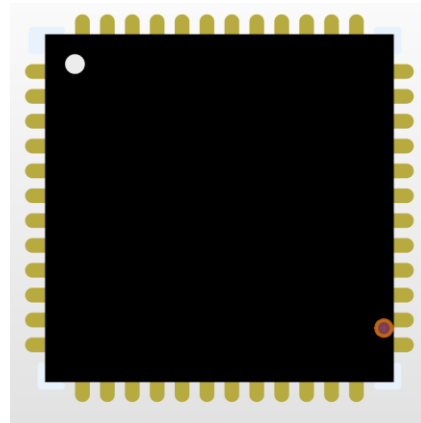
35	IDX	VDDIO	7
		VDDIO	29
2	I2C_SCL	VDD18_CSI	17
4	I2C_SDA	VDD18_P0	45
		VDD18_P1	36
37	MODE	VDD18_FPD0	40
30	PDB	VDD18_FPD1	31
		VDD11_D	3
48	LOCK	VDD11_CSI	20
46	VDD_SEL	VDD11_FPD1	34
		VDD11_FPD0	43
44	RES	RIN0+	41
6	BISTEN	RIN0-	42
47	PASS	RIN1+	32
		RIN1-	33
38	CMLOUTP	GPIO1	27
39	CMLOUTN	GPIO0	28
		GPIO2	26
24	CSI_D3P	GPIO3/INTB	25
23	CSI_D3N	GPIO4	24
22	CSI_D2P	GPIO5	23
21	CSI_D2N	GPIO6	22
16	CSI_D1P		
15	CSI_D1N		
14	CSI_D0P		
13	CSI_D0N	XOUT	4
12	CSI_CLK0P		
11	CSI_CLK0N	XIN/REFCLK	5
19	CSI_CLK1P		
18	CSI_CLK1N	GND_PAD	49

DS90UB954TRGZTQ1

Symbol



Footprint



3D Model

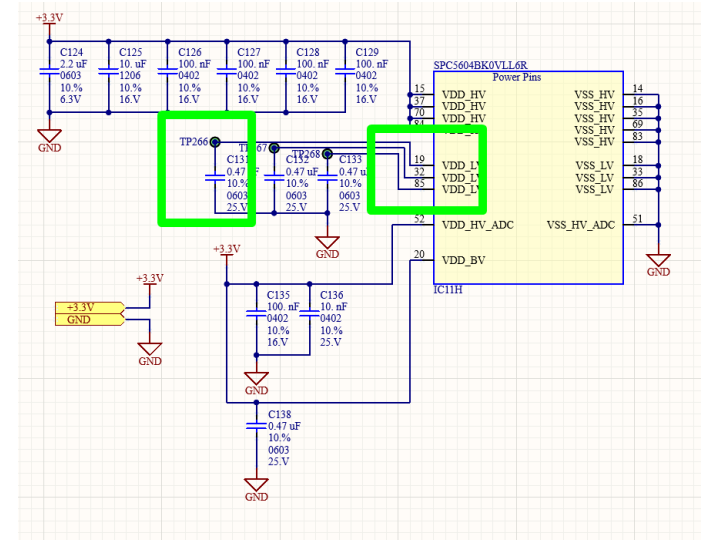
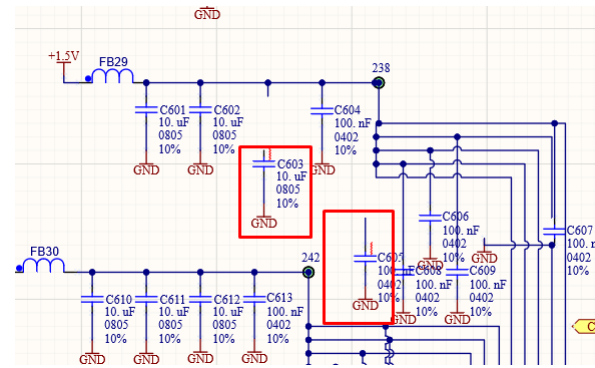
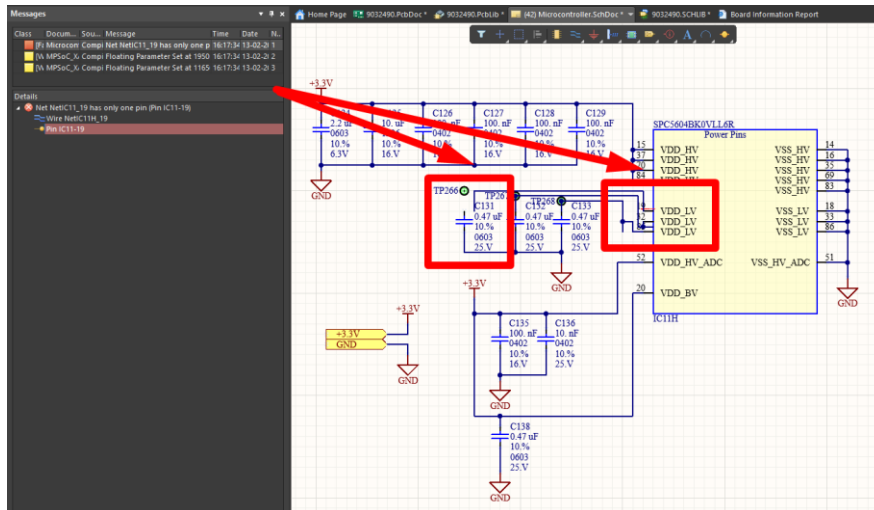
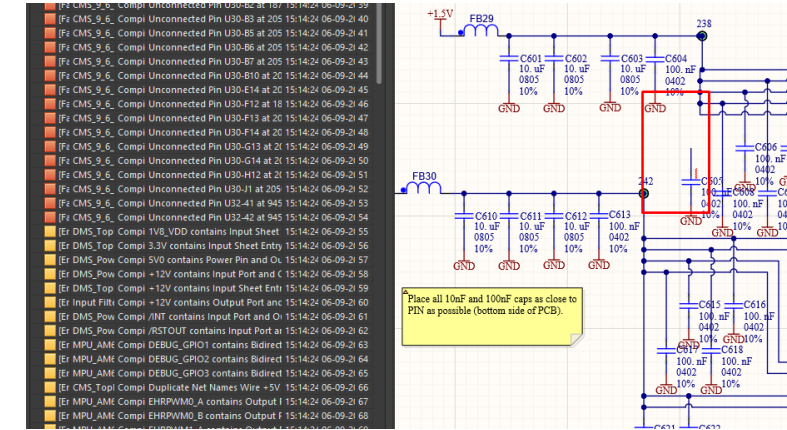
The library files, including symbols, footprints, and 3D models, will be reviewed to ensure they meet standards, with new libraries created as needed.

- **Verified:** 420 symbols and 260 footprints
- **Updated to Standards:** 40 symbols and 33 footprints
- **Created:** 20 new symbols and 32 new footprints



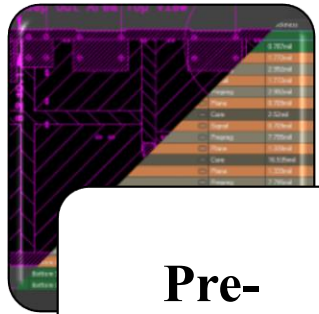
Schematic Review and Validation

- Developing a power flow diagram and block diagram based on the schematics.
- Manually checking net and port connections to eliminate any floating nets in the schematic.
- Correcting any errors found in the schematics.
- Performing verification through ERC (Electrical Rules Check).



PCB Layout Design

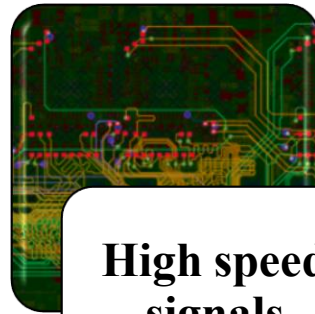
PCB Layout Design - Execution



**Pre-
Layout
Process**



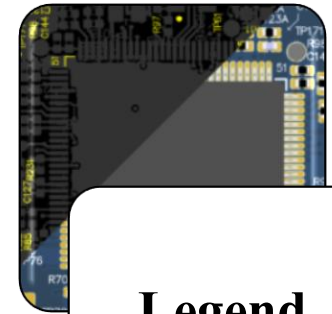
**Placement
and
Routing**



**High speed
signals
Length
Matching**



**DRC, Cu
Clean up**



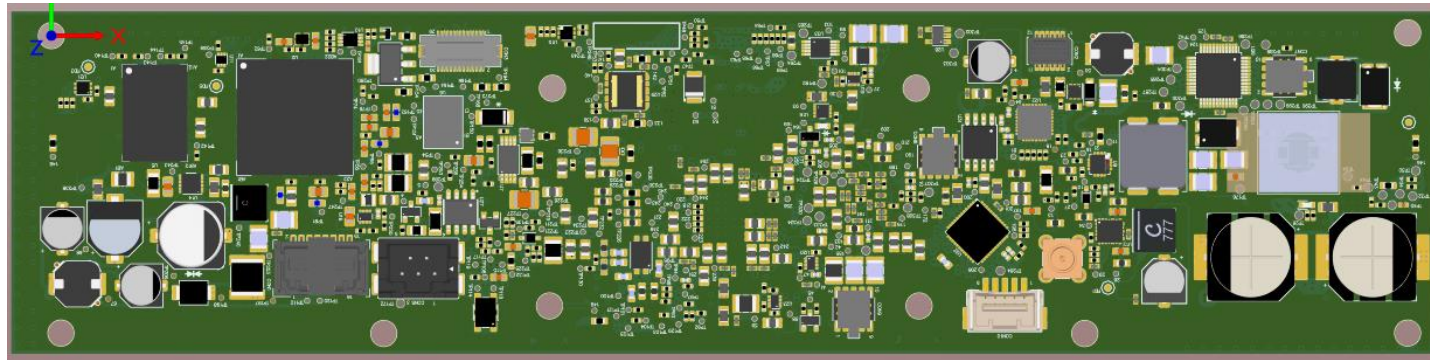
**Legend
cleanup**



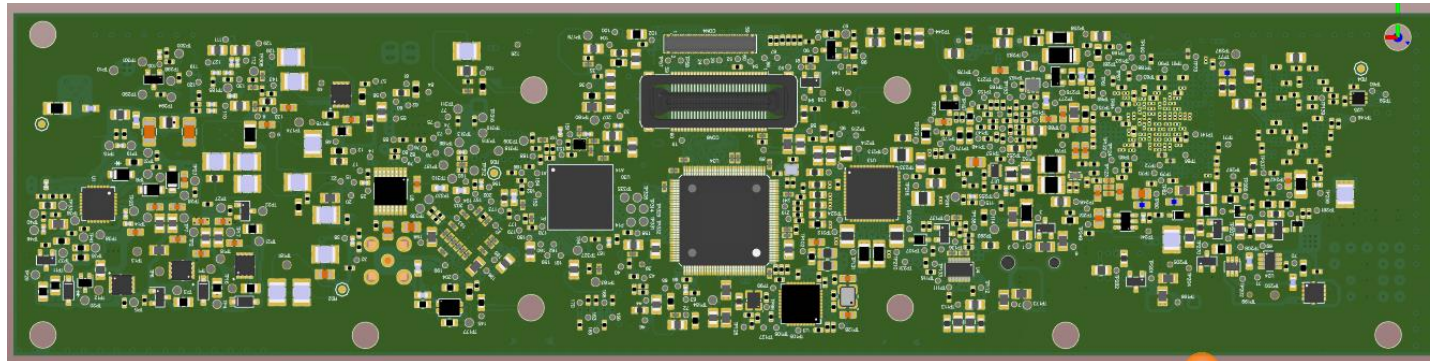
Results and Review

- Completed layout design with considerations for power distribution, EMI/EMC, and Design for Manufacturing
- Incorporated and verified client reviews and feedback at each stage of the design process.

Top view (3D)



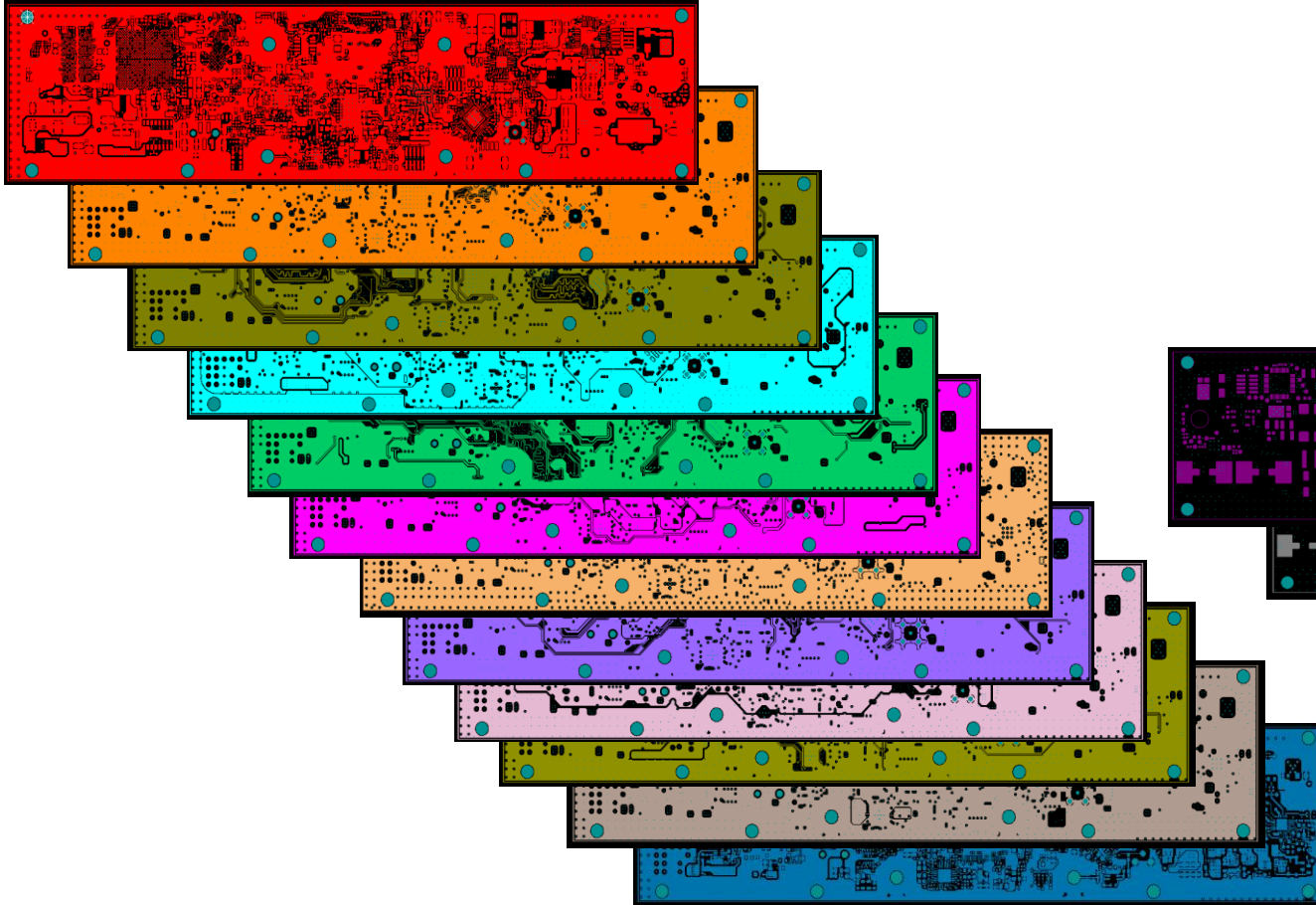
Rear view (3D)



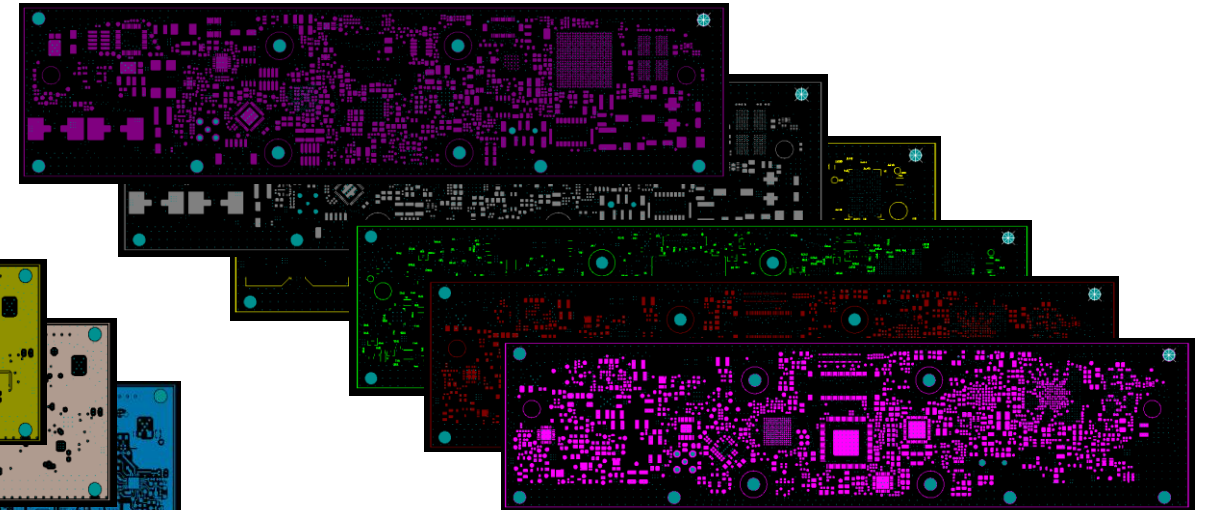
MFG Outputs Generation

MFG Outputs

- Gerber Files
- NC Drill Files.
- ODB++ files
- Hyper Lynx File



Copper Layers (Electrical)

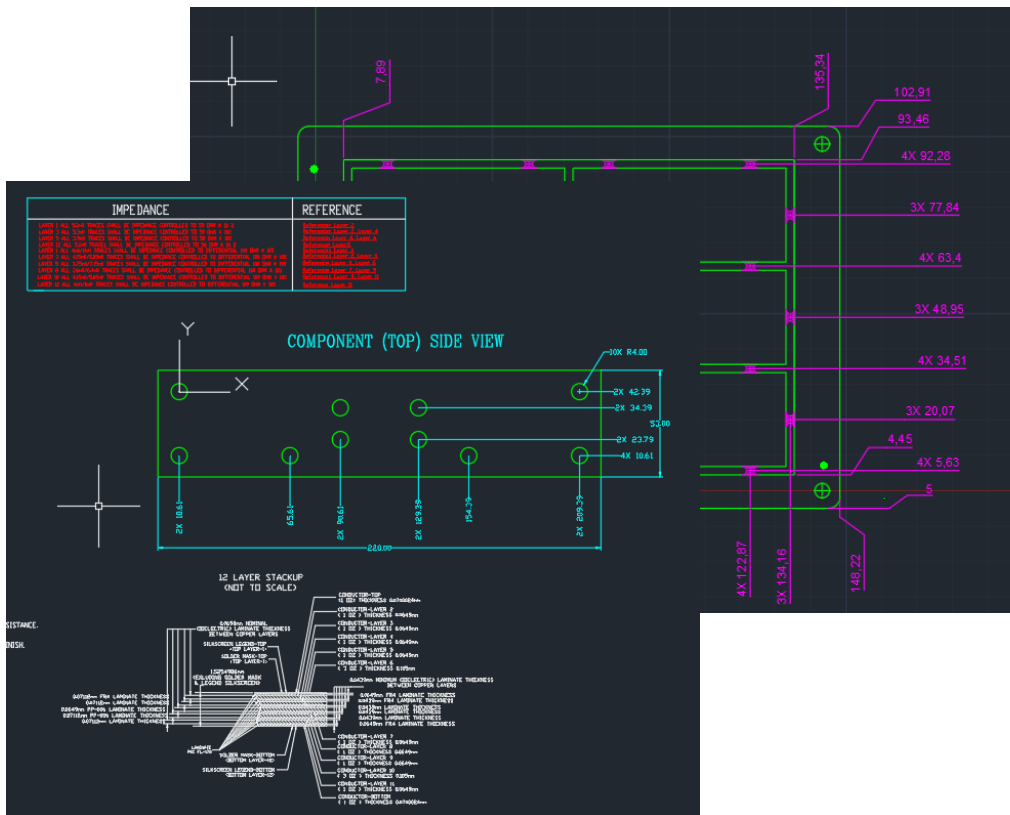


**Solder Mask, Solder paste &
Overlay Layers (Non-Electrical)**



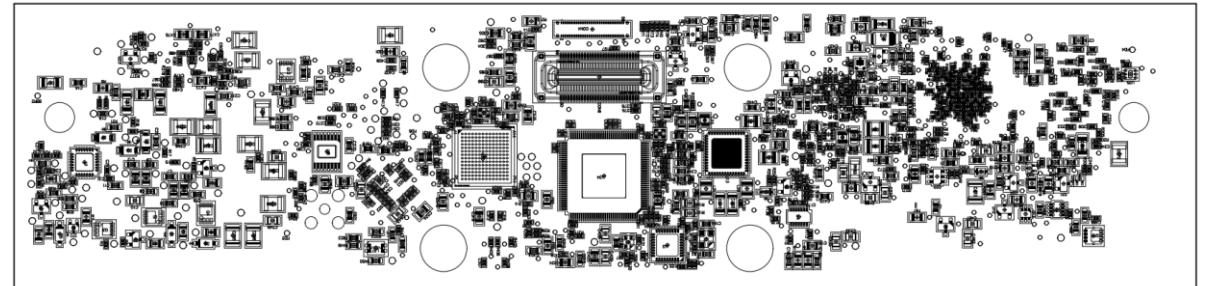
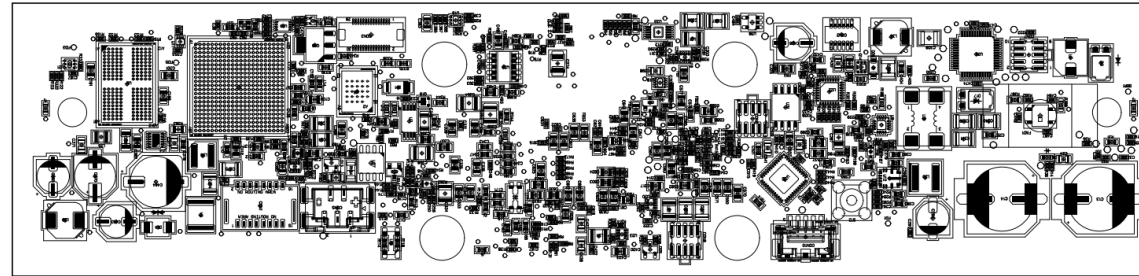
Fabrication Outputs Generation

- Fab and Array Drawings
- 3D step File



Assembly Outputs Generation

- BOM (Bill Of Materials) and PNP (Pick and Place) file
- Assembly Drawings (PDF file)

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A Heartfelt Customer's Voice

The testimonial is a glowing review, highlighting the great effectiveness of PCB design and its impressive result,

"Collaborating with the GigHz team on our PCB design was a transformative experience. Their commitment to solving challenges, maintaining precision, and delivering a top-tier design within the timeframe and cost was remarkable. The final PCB not only met our technical needs but surpassed our expectations. Their expertise, passion, and dedication to quality were evident at every stage. We look forward to working with them again and highly recommend their exceptional services!"



Conclusion

- Designing the board presented challenges, particularly in managing a high number of connections within a compact space.
- Achieving the desired impedance profile for various signals required a strong focus on precision and quality.
- Leveraging our PCB design expertise, we efficiently overcame obstacles while upholding high quality standards.
- We proudly delivered a high-quality PCB that met technical requirements, adhered to timelines and budgets, and earned customer approval.

