Signal Integrity Analysis
Autonomous Valet Parking System

Scope : Signal Integrity Analysis

Application : Advanced Driver Assistance System (ADAS)

Signal integrity is essential for Autonomous Valet Parking (AVP) systems within Advanced Driver Assistance Systems (ADAS). AVP relies on precise electronic communication via sensors, cameras, and software to autonomously identify and navigate parking spaces, and to control vehicle dynamics such as steering, acceleration, and braking. This technology enables seamless, efficient parking, enhancing convenience and safety by allowing drivers to leave their vehicles at the entrance of a parking facility while the system handles the parking process.

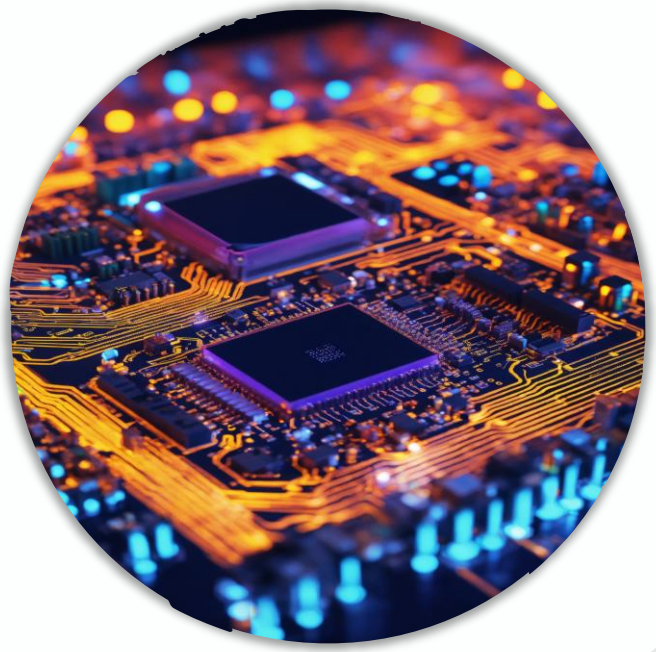
Signal Integrity Analysis - Challenges

The client has requested a signal integrity analysis of the layout to ensure its performance. The following highlights the key technical challenges associated with this analysis.

Challenges

- Signal Degradation
- Crosstalk
- Timing Variations and Jitter
- Impedance Matching
- Signal Attenuation
- Via and Connector Impedance
- Trace Routing and Layout Challenges
- Return Path Issues
- Power Distribution Network
- Continuous Reference Planes
- Noise and Electromagnetic Interference (EMI)

Signal Integrity Analysis - SoW



Study of High Speed Signals/Groups
Impedance and Requirements listing

Analysis Execution
Required Parameters for analysis

Analysis – Performance Evaluation
Plots and Results

Layout Recommendations
To enhance Performance

Layout Implementations
Modifications in Layout design

Study of High Speed Signals / Groups

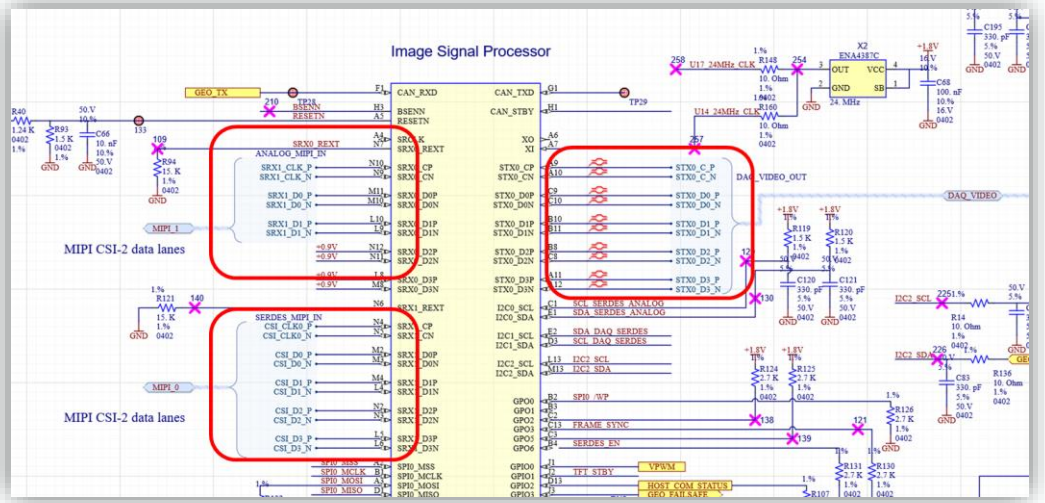
The High Speed Signal circuits in the project are studied thoroughly to evaluate the performance.

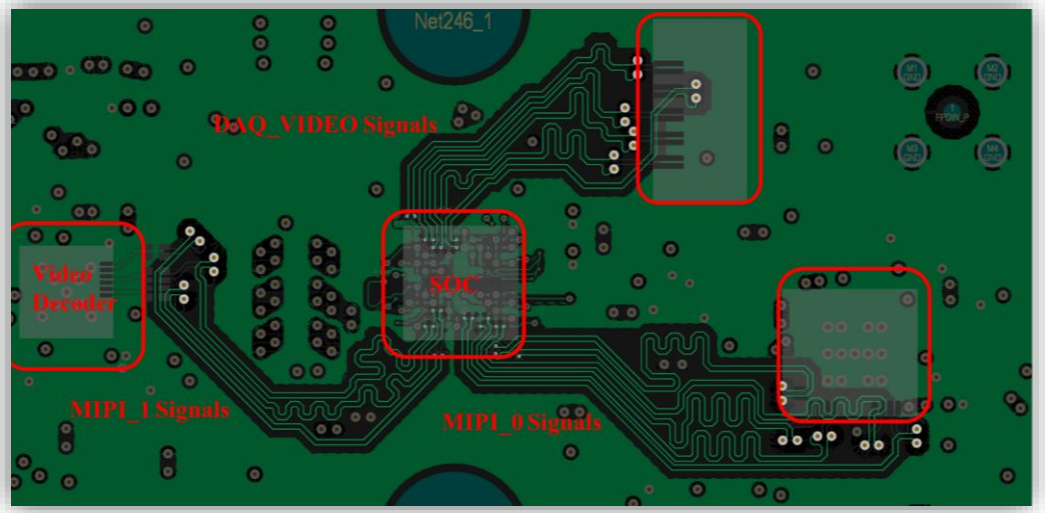
High Speed Signals

- MIPI_0 – De-serializer to SoC
- MIPI_1 – Video Decoder to SoC
- DAQ_VIDEO – SoC to Expansion Connector

High Speed Signal Circuits

- De-serializer
- SOC
- Video Decoder





Analysis Execution

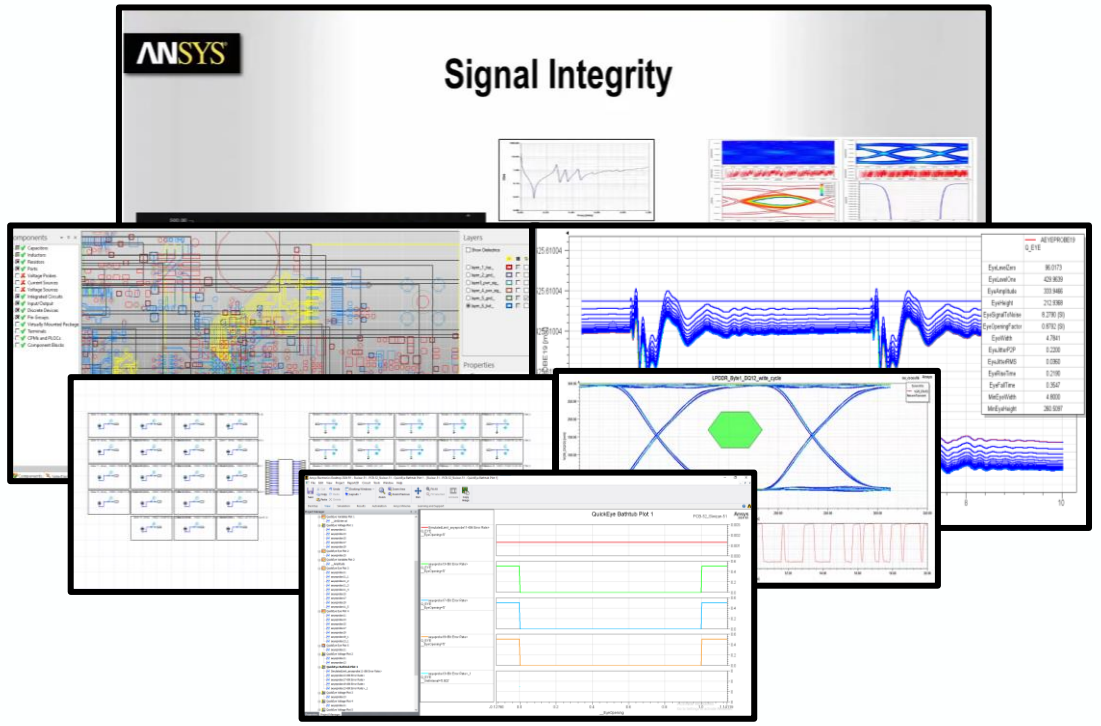
We executed the analysis in **Ansys-SI Wave** tool, to evaluate the signal integrity performance of the layout.

Problems of Signal Integrity is identified from two levels:

- Interconnect level
- Systems-level

Quantities to calculate include:

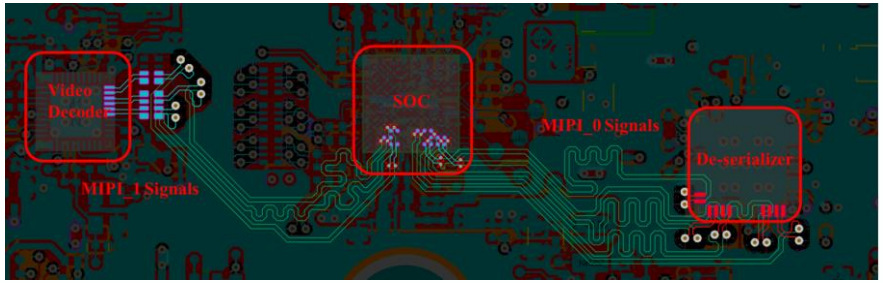
- ✓ Edge Rate
- ✓ Characteristic Impedance
- ✓ Signal-to-Noise Ratio (SNR) Margin
- ✓ Timing Skew
- ✓ Simultaneous Switching Noise Impact



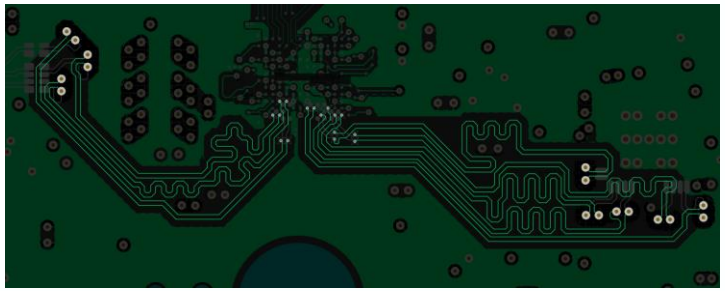
Analysis Execution (Cont.)

MIPI signals – MIPI_0 – De-serializer to SoC
MIPI_1 – Video Decoder to SoC

Layout - Routing



Layer 5

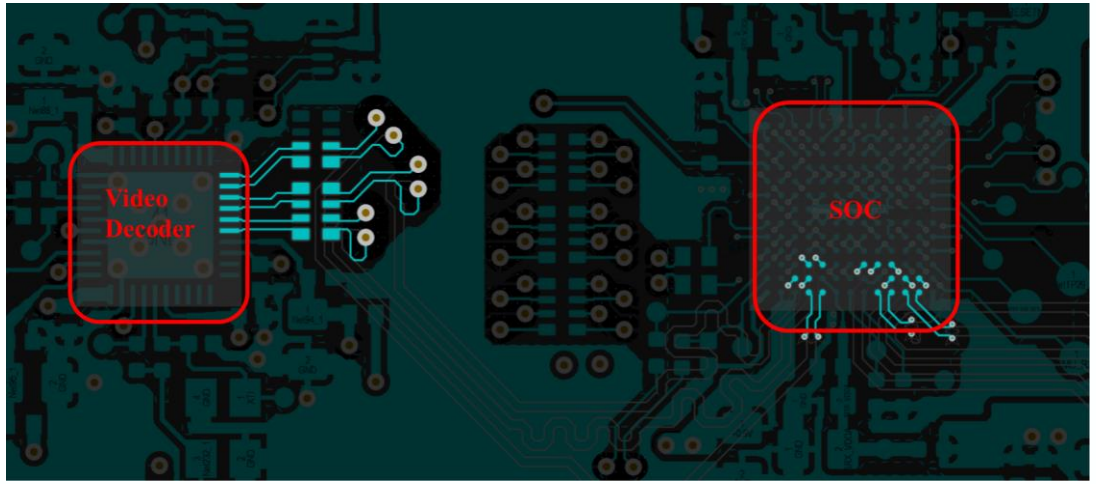


Trace Lengths

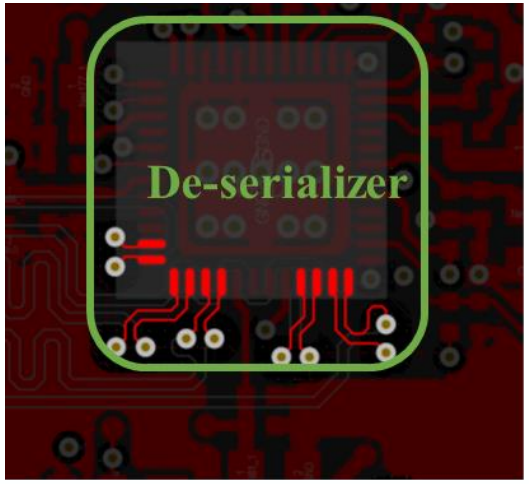
Name	Node ...	Signal Le...	Total Pin...	Routed L...	Unroute...
MIPI_1.SRX1_CLK_N-CK_N	4	1494.551	0	1494.551	0
MIPI_1.SRX1_CLK_P-CK_P	4	1494.551	0	1494.551	0
MIPI_1.SRX1_D0_N-D0_N	4	1494.428	0	1494.428	0
MIPI_1.SRX1_D0_P-D0_P	4	1494.428	0	1494.428	0
MIPI_1.SRX1_D1_N-D1_N	4	1494.428	0	1494.428	0
MIPI_1.SRX1_D1_P-D1_P	4	1494.428	0	1494.428	0

Name	Nod...	Signal Leng...	Total...	Routed Len...	Unrout...
MIPI_0.CSI_CLK0_N	2	1635.264	0	1637.228	0
MIPI_0.CSI_CLK0_P	2	1635.264	0	1636.838	0
MIPI_0.CSI_D0_N	2	1635.141	0	1636.325	0
MIPI_0.CSI_D0_P	2	1635.141	0	1637.832	0
MIPI_0.CSI_D1_N	2	1635.141	0	1636.327	0
MIPI_0.CSI_D1_P	2	1635.141	0	1636.325	0
MIPI_0.CSI_D2_N	2	1635.141	0	1636.325	0
MIPI_0.CSI_D2_P	2	1635.141	0	1636.325	0
MIPI_0.CSI_D3_N	2	1635.141	0	1636.325	0
MIPI_0.CSI_D3_P	2	1635.141	0	1636.325	0

Layer 6



Layer 1

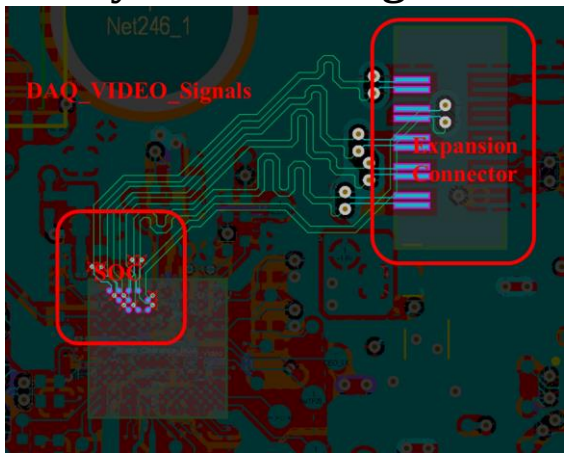


CLK and Data's are routed with same trace length (closely)

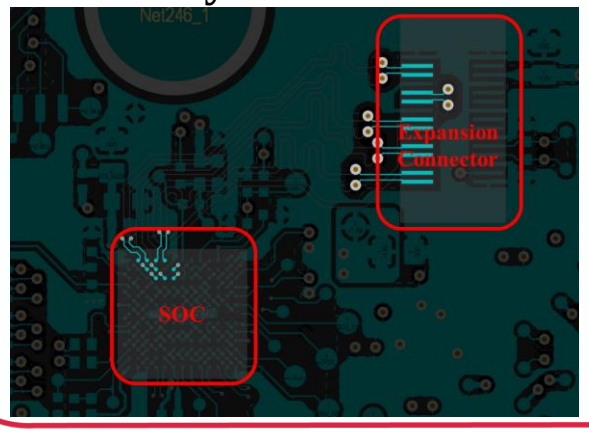
Analysis Execution (Cont.)

DAQ_VIDEO – SoC to Expansion Connector

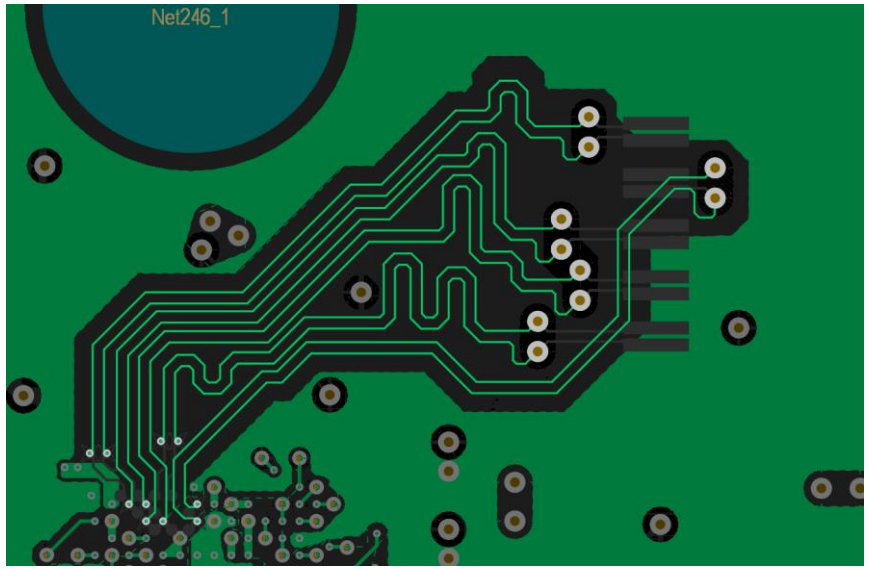
Layout - Routing



Layer 6



Layer 3



Trace Lengths

Name	Node...	Signal Lengt...	Total ...	Routed Leng...	Unrouted...
DAQ_VIDEO.STX0_C_N	2	1047.723	0	1049.137	0
DAQ_VIDEO.STX0_C_P	2	1047.723	0	1049.082	0
DAQ_VIDEO.STX0_D0_N	2	1047.6	0	1049.014	0
DAQ_VIDEO.STX0_D0_P	2	1047.6	0	1049.014	0
DAQ_VIDEO.STX0_D1_N	2	1047.6	0	1049.015	0
DAQ_VIDEO.STX0_D1_P	2	1047.6	0	1049.014	0
DAQ_VIDEO.STX0_D2_N	2	1047.6	0	1048.558	0
DAQ_VIDEO.STX0_D2_P	2	1047.6	0	1048.559	0
DAQ_VIDEO.STX0_D3_N	2	1047.6	0	1049.121	0
DAQ_VIDEO.STX0_D3_P	2	1047.6	0	1049.122	0

CLK and Data's are routed with same trace length (closely)

Analysis - Plots and Results (Cont.)

Topology – MIPI_0 – CLK & DATA

Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 760 mV

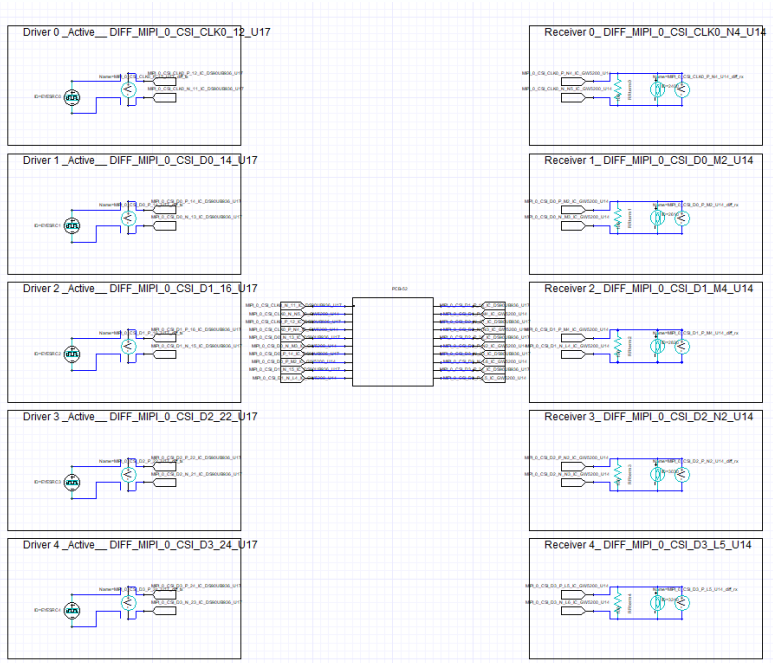
VinL = 580 mV

High Speed Mode:

VinH = 480 mV

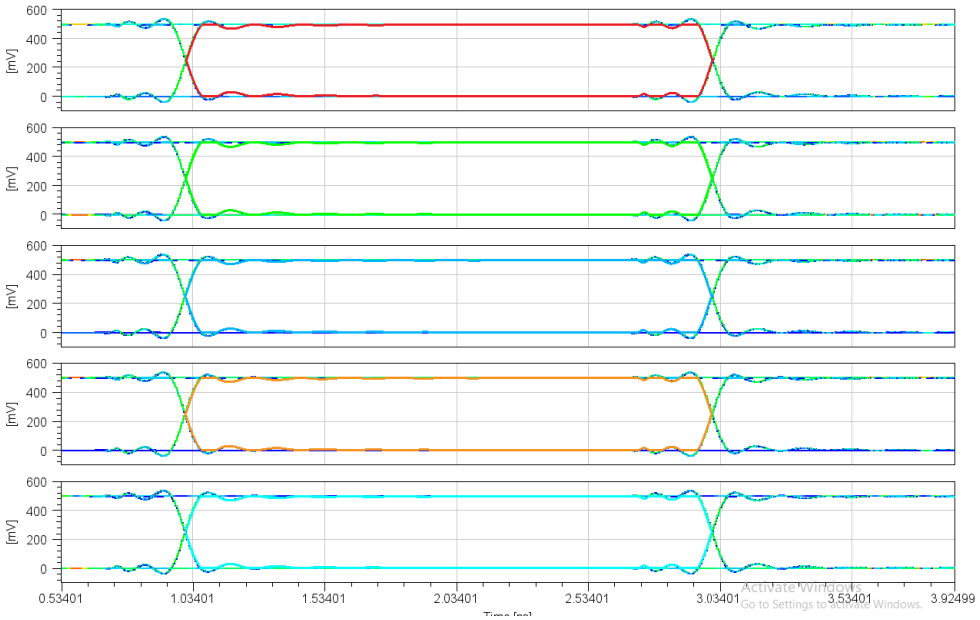
VinL = 45 mV

Circuit in AEDT



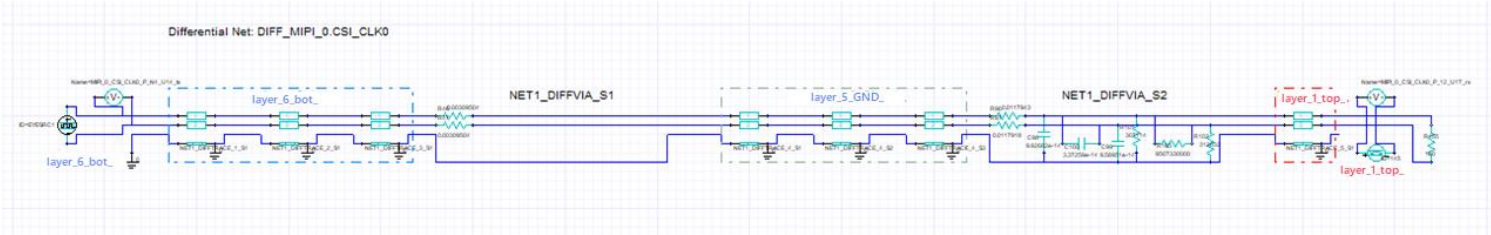
Analysis Result

Quick-Eye Plot View



Both the values are meeting the requirement and the results are **pass.**

Analysis - Plots and Results



Topology – MIPI_1 - CLK

Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 760 mV

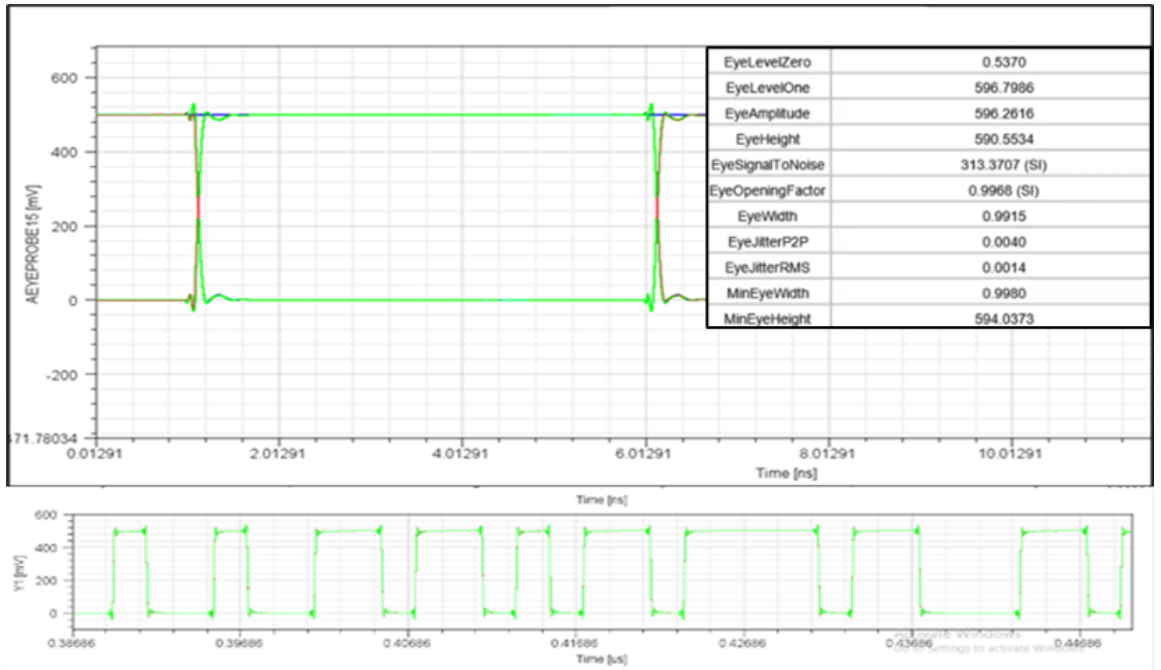
VinL = 580 mV

High Speed Mode:

VinH = 480 mV

VinL = 45 mV

Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Analysis - Plots and Results (Cont.)

Topology – DAQ_VIDEO- CLK & DATA

Analysis Parameters – Requirements

As per SoC,

V_{OH} = 1600mV

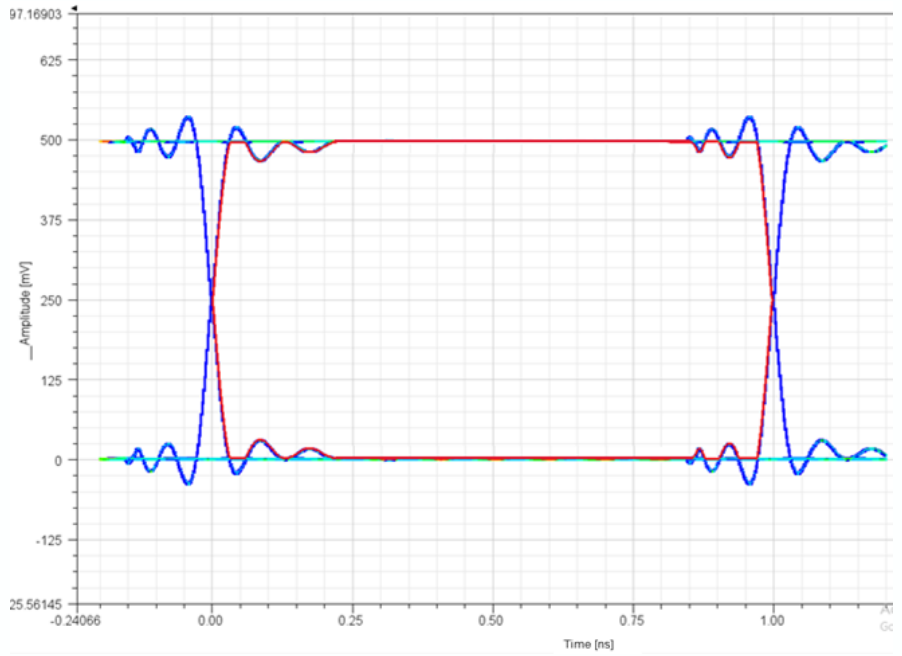
V_{OL} = 800mV

Signal Net Delay Report

Net	Length (mm)	Differential Pair Length Mismatch (mm)	Delay (ps)	Differential Pair Delay Mismatch (ps)
DAQ_VIDEO.STX0_C_P (Differential Net: DIFF_DAQ_VIDEO.STX0_C (DAQ_VIDEO.STX0_C_P and DAQ_VIDEO.STX0_C_N))	25.721	0.000	177.224	-0.294
DAQ_VIDEO.STX0_C_N (Differential Net: DIFF_DAQ_VIDEO.STX0_C (DAQ_VIDEO.STX0_C_P and DAQ_VIDEO.STX0_C_N))	25.721	-0.000	177.518	0.294
DAQ_VIDEO.STX0_D0_P (Differential Net: DIFF_DAQ_VIDEO.STX0_D0 (DAQ_VIDEO.STX0_D0_P and DAQ_VIDEO.STX0_D0_N))	25.718	0.000	172.158	-6.106
DAQ_VIDEO.STX0_D0_N (Differential Net: DIFF_DAQ_VIDEO.STX0_D0 (DAQ_VIDEO.STX0_D0_P and DAQ_VIDEO.STX0_D0_N))	25.718	-0.000	178.264	6.106
DAQ_VIDEO.STX0_D1_P (Differential Net: DIFF_DAQ_VIDEO.STX0_D1 (DAQ_VIDEO.STX0_D1_P and DAQ_VIDEO.STX0_D1_N))	25.718	0.000	172.300	-6.217
DAQ_VIDEO.STX0_D1_N (Differential Net: DIFF_DAQ_VIDEO.STX0_D1 (DAQ_VIDEO.STX0_D1_P and DAQ_VIDEO.STX0_D1_N))	25.718	-0.000	178.517	6.217
DAQ_VIDEO.STX0_D2_P (Differential Net: DIFF_DAQ_VIDEO.STX0_D2 (DAQ_VIDEO.STX0_D2_P and DAQ_VIDEO.STX0_D2_N))	25.718	0.000	177.681	-0.578
DAQ_VIDEO.STX0_D2_N (Differential Net: DIFF_DAQ_VIDEO.STX0_D2 (DAQ_VIDEO.STX0_D2_P and DAQ_VIDEO.STX0_D2_N))	25.718	-0.000	178.259	0.578
DAQ_VIDEO.STX0_D3_P (Differential Net: DIFF_DAQ_VIDEO.STX0_D2 (DAQ_VIDEO.STX0_D3_P and DAQ_VIDEO.STX0_D3_N))	25.718	0.000	177.681	-0.578
DAQ_VIDEO.STX0_D3_N (Differential Net: DIFF_DAQ_VIDEO.STX0_D2 (DAQ_VIDEO.STX0_D3_P and DAQ_VIDEO.STX0_D3_N))	25.718	-0.000	178.259	0.578

From the above net delay report, DAQ_VIDEO signal groups delay mismatch is within tolerance (ps).

Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Layout Recommendations

The PCB layout's performance can be increased by the following recommendations

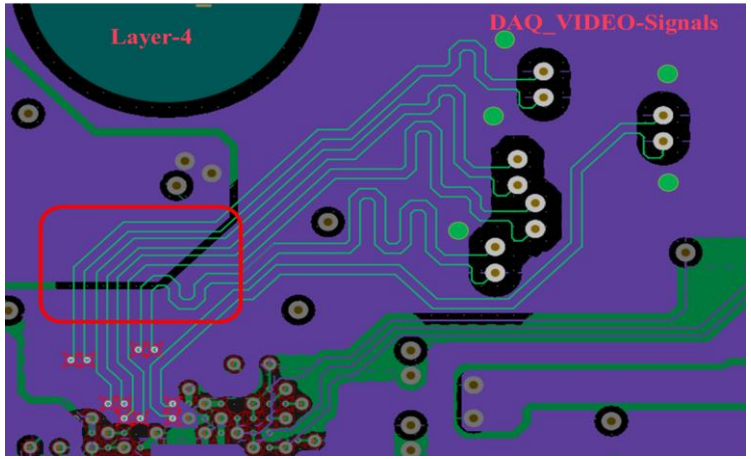
1. Increase the spacing between high speed signal traces and GND polygon.

   5H (5 x 5= 25 mils)

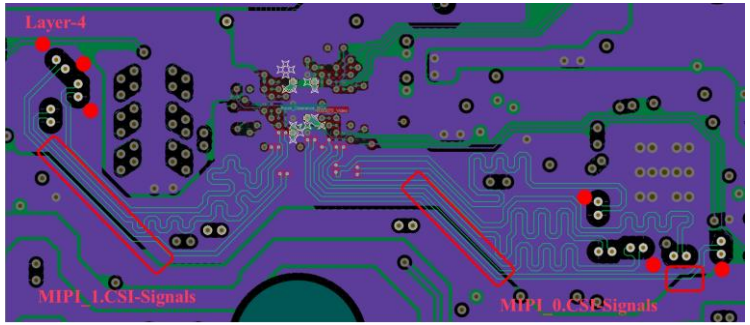
2. Give proper **GND reference** plane for the high speed signal traces. Try to give **sandwich reference** plane for these signals.

3. Add GND Vias near the Signal Layer Switching Vias.

4. Use **arc routing** is preferred over **45-degree** angles for high-speed signals to reduce impedance discontinuities and signal reflections, enhancing signal integrity and performance."



Place Vias



Place Vias

Layout Implementations

Suggested recommendations are incorporated to the PCB layout to enhance its performance.

MIPI Signals: MIPI_0 – De-serializer to SoC
MIPI_1 – Video Decoder to SoC

Clearance:

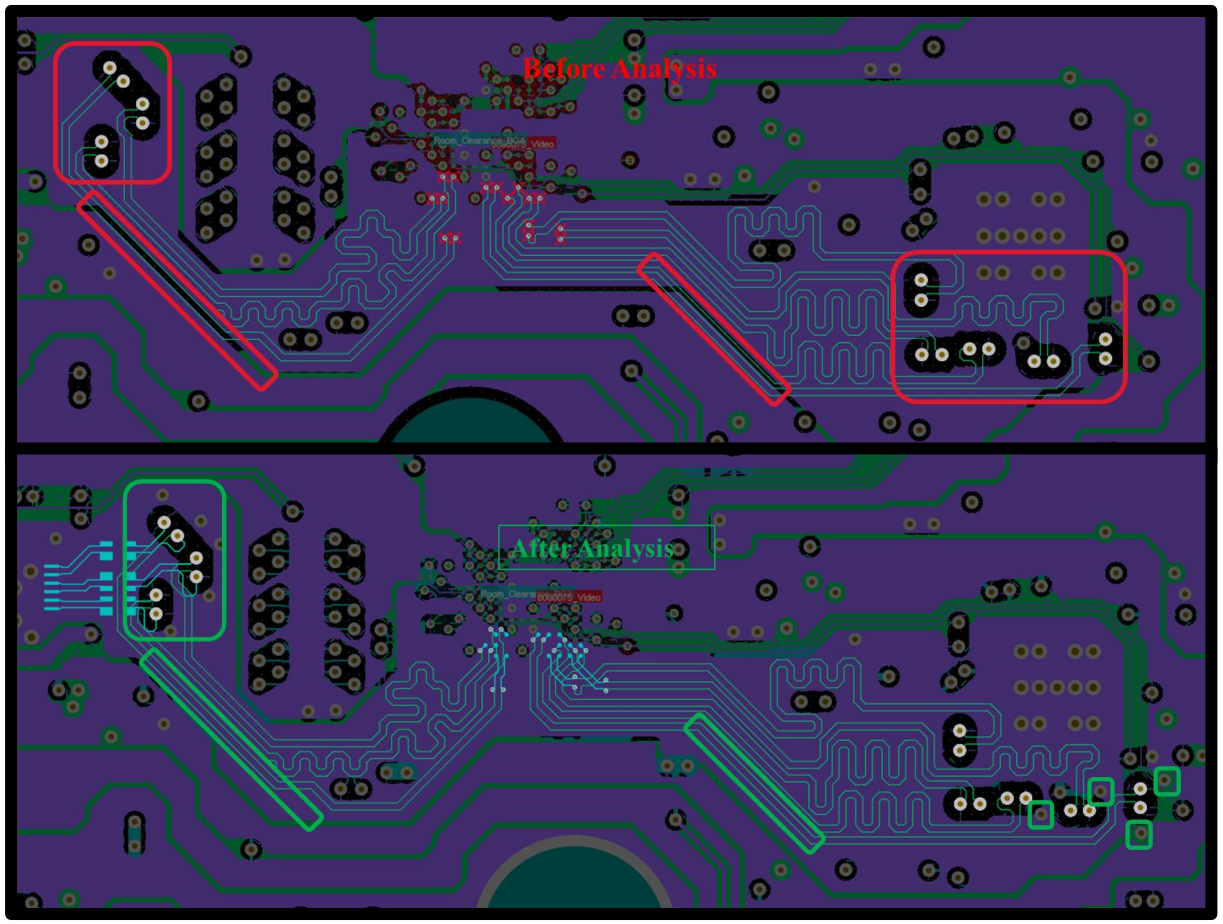
Routing optimized to increase the spacing (5H - 25 mils) between GND and MIPI signal traces.

Vias:

GND vias are placed near to the switching places of the Signal traces.

Reference Plane:

Proper GND reference plane are provided for high speed signals in Layer-4.



Layout Implementations (Cont.)

DAQ_VIDEO Signals : SOC to Expansion Connector

Clearance:

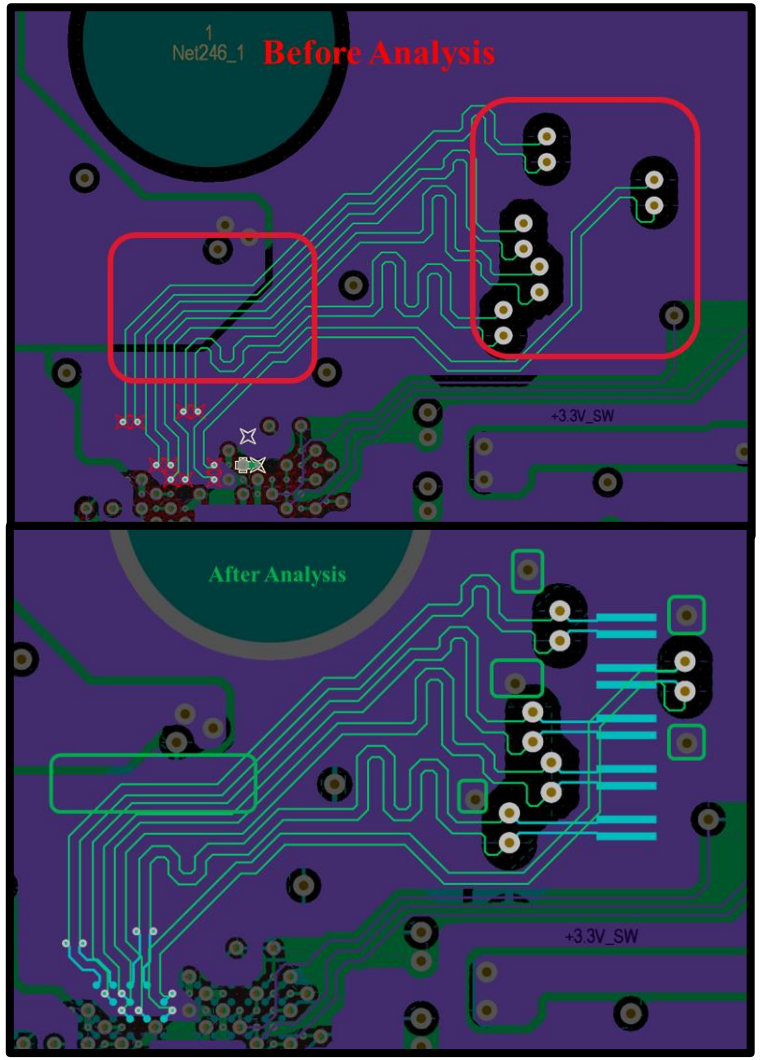
Routing optimized to increase the spacing between GND and DAQ_VIDEO signal traces.

Vias:

GND vias are placed near to the switching places of the Signal traces.

Reference Plane:

Proper GND reference plane are provided for high speed signals in Layer-4.



Customer Testimonial

Delighted to share a testimonial from a distinguished client, highlighting the outstanding success and significant benefits of our Signal Integrity Analysis.

"Engaging the team for Signal Integrity (SI) Analysis revolutionized our project. Their meticulous approach ensured superior quality by identifying potential issues and providing effective solutions. The detailed insights gained during the analysis were invaluable, significantly contributing to our project's overall success. Their cost-effective modifications to copper pours highlighted their dedication to resource optimization, while their timely delivery showcased their efficiency. We are extremely satisfied with the quality and promptness of the SI analysis, which has greatly enhanced the reliability and efficiency of our electronic design."

Conclusion

- We delivered a comprehensive set of recommendations to enhance high-speed signal performance and implemented layout design changes to improve overall efficiency, underscoring our commitment to high-quality work and technical expertise.
- Our collaboration transcends technical execution; it includes optimizing signal performance in the layout by leveraging our expertise and deep understanding of the client's specific requirements.
- Our dedication to delivering top-tier analysis services highlights our exceptional skills and unwavering reliability in achieving outstanding results.