Enhancing PCB Design for EMI/EMC Compliance

Scope: EMI/EMC Mitigation in PCB Design

Application: Advanced Driver Assistance Systems

The Blindspot Monitoring System is an extra set of watchful eyes while driving. Blind Zone Indicators (BZIs) represent a category of Advanced Driver Assistance Systems (ADAS), this clever technology helps you avoid accidents by detecting cars or objects in those tricky blind spots beside your vehicle. Using sensors, cameras, and alerts, Blind Zone Indicators inform drivers about objects or vehicles hidden in their blind spots, which are not visible through rearview or side mirrors, thereby helping to prevent accidents.

EMI/EMC Compliance - Challenges

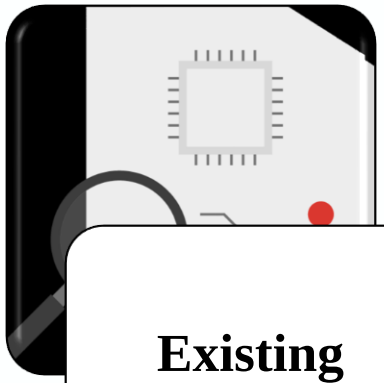
The client has approached us to reduce the output noise caused by Electromagnetic Interference (EMI) and address Electromagnetic Compatibility (EMC) issues on their PCB.

Challenges:

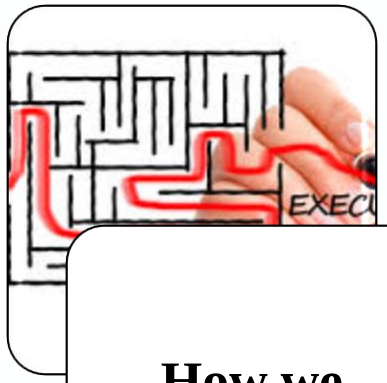
- Ensure design changes do not affect the image signal group on the PCB.
- Minimize output data noise to enhance signal integrity.
- Avoid high-level design changes.
- Exclude the addition of major IC components to address these issues.
- Mitigate Electromagnetic Interference (EMI) and ensure Electromagnetic Compatibility (EMC) on the PCB.
- Adhere to a tight project completion timeline

Design Optimization-SoW

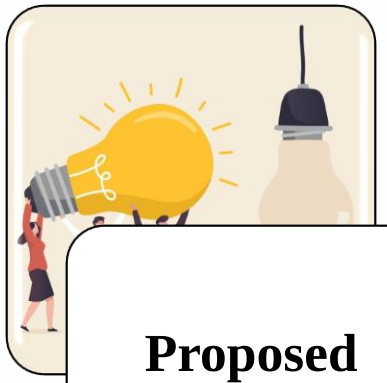
Existing Schematic Review



Existing Layout Inspection

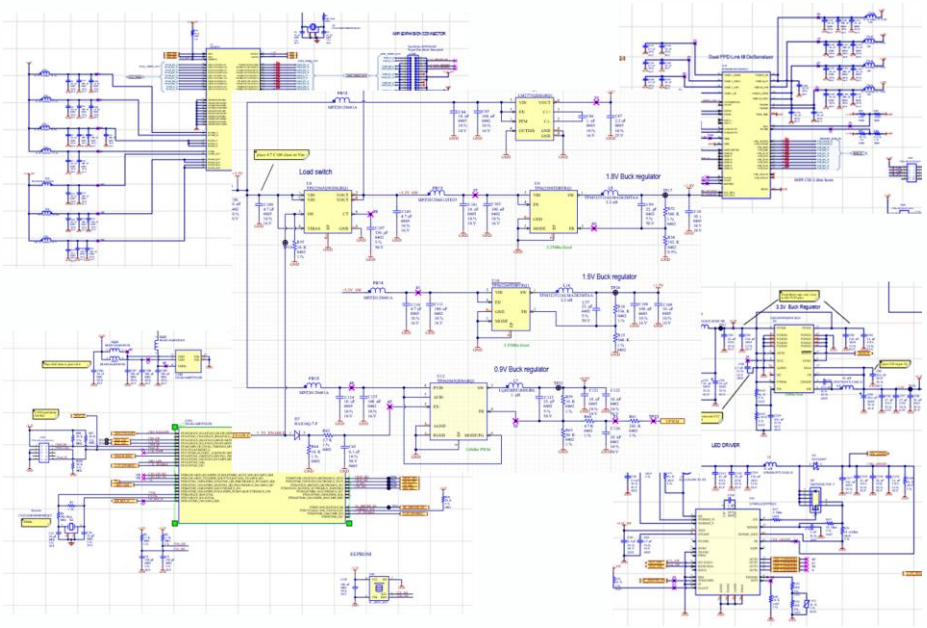


How we executed?



Proposed Design & Suggestion

Existing Schematic Review



These points were reviewed during schematic Review to ensure that the product met EMI/EMC requirements and operated reliably in its intended environment.

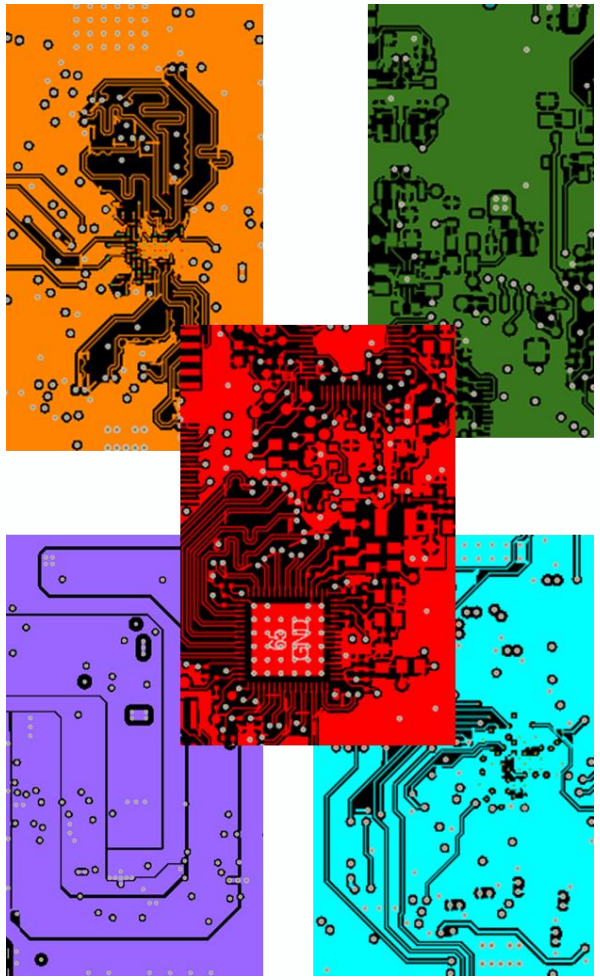
Schematic Level Review Points for EMI/EMC Analysis

- **Component Selection:**
  - Use EMI/EMC-compliant components with built-in suppression.
- **Power Supply Decoupling:**
  - Include decoupling capacitors for each IC and select appropriate values.
- **Filter Components:**
  - Add ferrite beads, chokes, and EMI filters; ensure proper values and placement.
- **Clock Management:**
  - Ensure correct clock signal handling and include termination resistors.
- **I/O Port Design:**
  - Use filtering and protection components; include TVS diodes if needed.
- **Documentation and Compliance:**
  - Ensure the schematic meets EMI/EMC standards and document design choices.

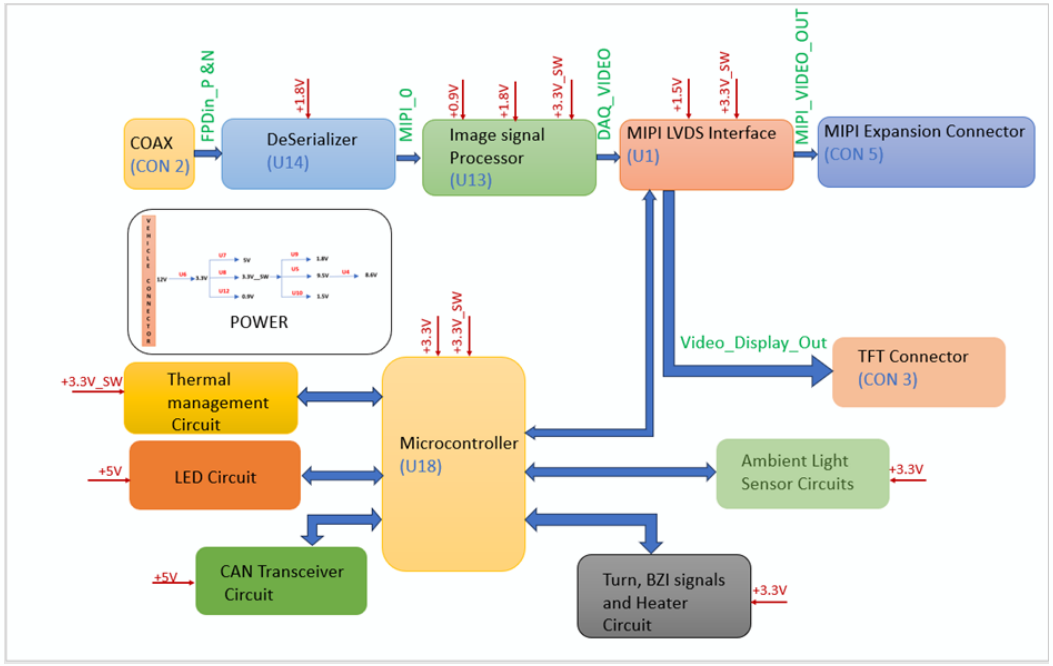
Existing Layout Inspection

PCB Layout Level Review Points for EMI/EMC Analysis

- **Component Placement**:
  - ✓ Position high-speed and sensitive components to minimize noise and interference.
- **Grounding and Ground Planes:**
  - ✓ Implement a continuous ground plane and avoid ground loops.
- **Trace Routing:**
  - ✓ Keep high-frequency traces short and avoid routing over gaps. Route sensitive signals away from noisy areas.
- **Power Supply Decoupling:**
  - ✓ Place decoupling capacitors near IC power pins and verify their values.
- **PCB Layer Stack-Up:**
  - ✓ Use a multilayer design with dedicated power and ground planes to ensure signal integrity and reduce EMI.
- **Signal Integrity:**
  - ✓ Maintain controlled impedance and use differential pairs where needed. Match trace lengths for differential signals.
- **Shielding:**
  - ✓ Apply and ground shielding for high-frequency components and traces.
- **Clock Management**:
  - ✓ Minimize clock trace lengths, use proper termination, and shield clock signals.

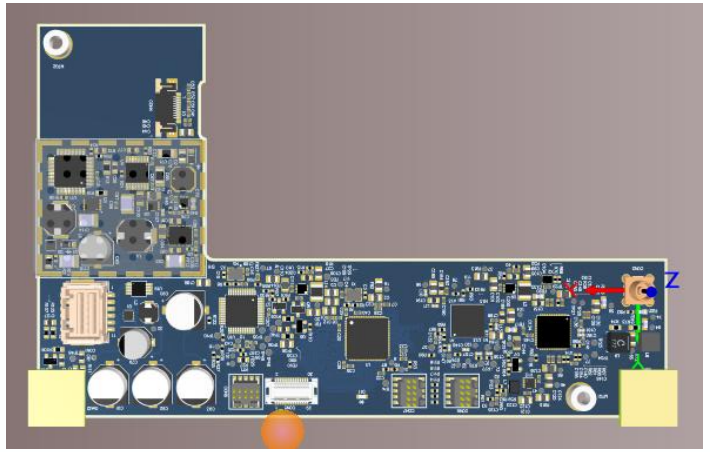


Project Objective



- In this project, a microcontroller teams up with an array of advanced sensing circuits, including the image signal processor circuits.
- An image signal is received through a coax connector and undergoes processing with a specialized component, De-Serializer (U14). Once processed, the image signal is transmitted to various connectors like TFT and MIPI Expansion Connector via the MIPI LVDS interface (U1). This enables the project to utilize the processed image signal for a wide range of applications, showcasing its versatility and technological appeal.

- The design outputs display unexpected fluctuations, with considerable noise affecting the output. This noise could potentially compromise the system's performance and reliability.



How we executed?

Upon reviewing the schematics and PCB of the existing project, several design aspects have been identified across various levels to minimize unwanted noise at output.

Schematic Design level

PCB Layout Design level

EMC shielding (Components level)

Design level (Schematics)

To reduce power rail noise and manage voltage fluctuations, **Decoupling capacitors** have been added based on the datasheet recommendations.

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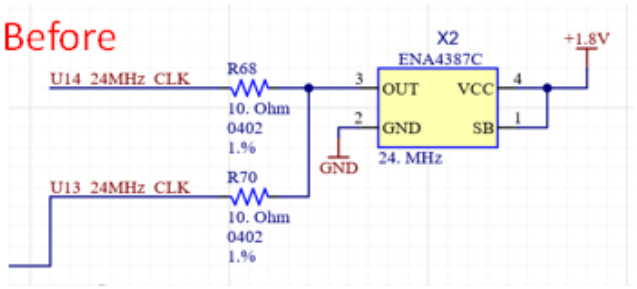

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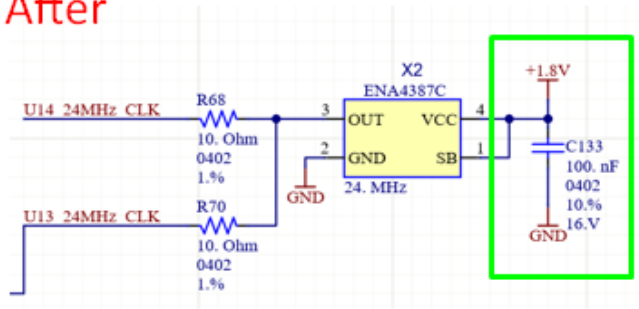

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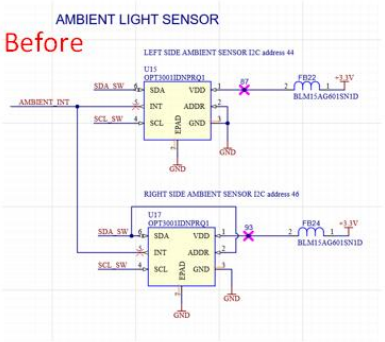

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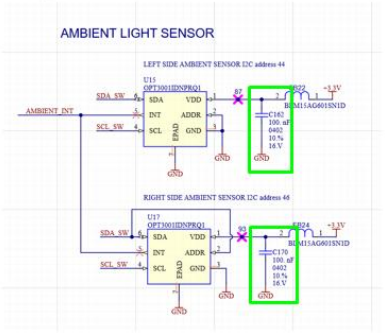

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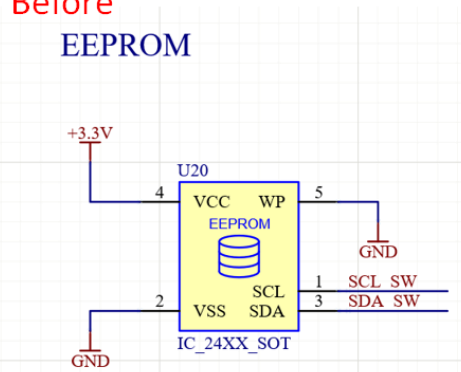

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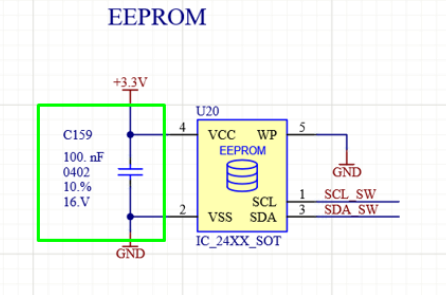
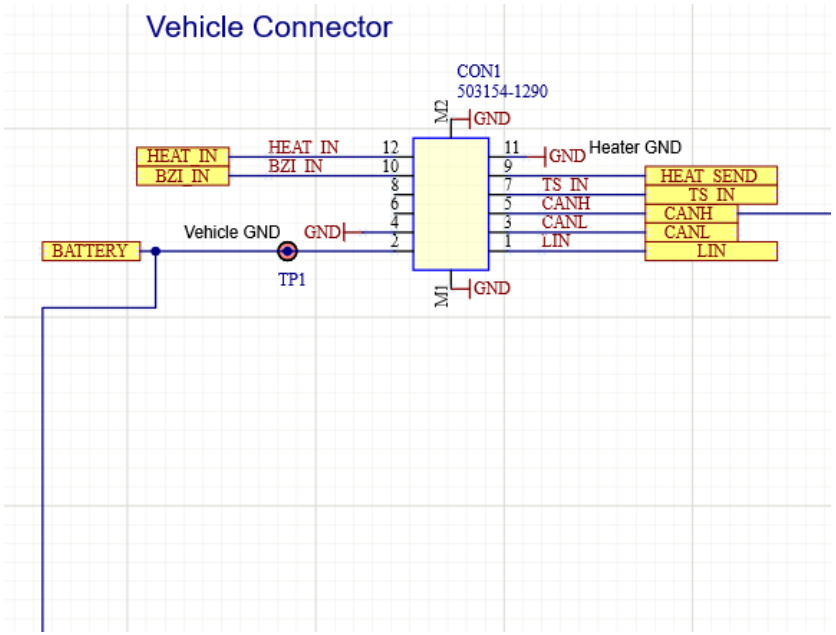


These Decoupling capacitors ***placed close to the IC power pins*** *and grounded directly to the ground planes.*

Design level (Schematics)

TVS diode and **parallel capacitors** were installed at the board's power entry **connector to mitigate voltage spikes and enhance power supply stability**.

Before



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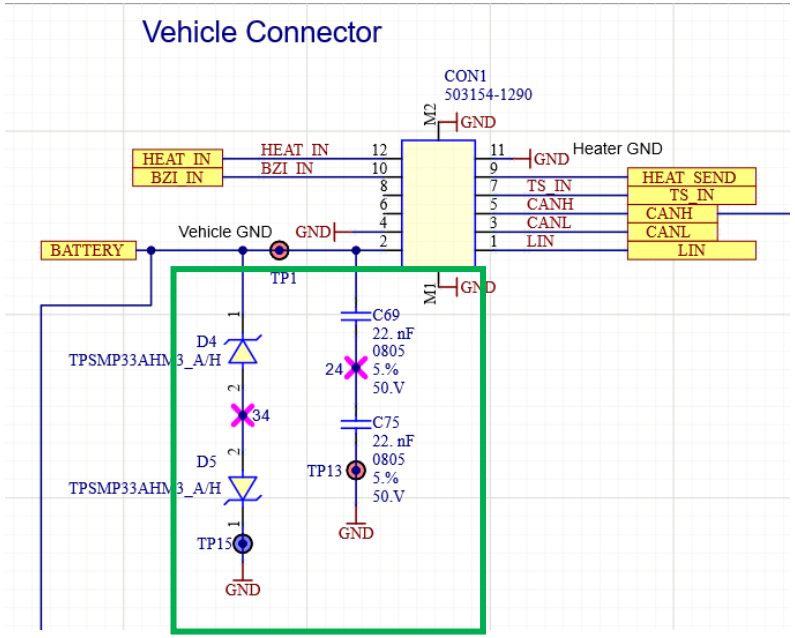

*These components were strategically **placed near the connector** in the PCB layout.*

Design level (PCB Layout)(Cont.)

GND vias were strategically placed along **LED anode and cathode traces** to ensure **effective grounding** and to optimize **signal integrity** and **noise reduction** throughout the circuit board layout.

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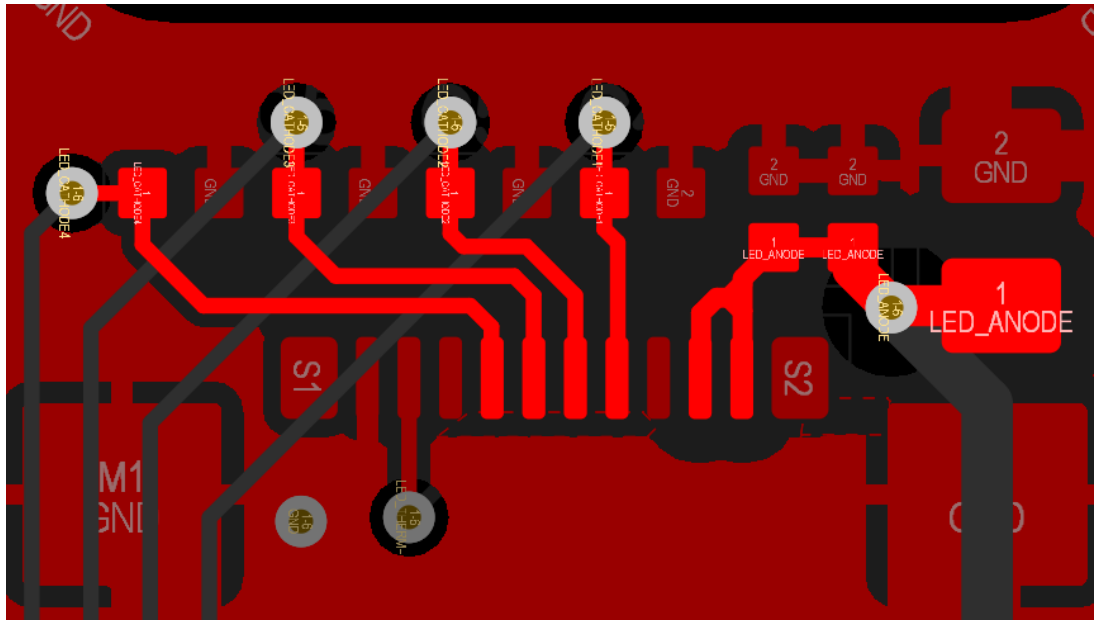

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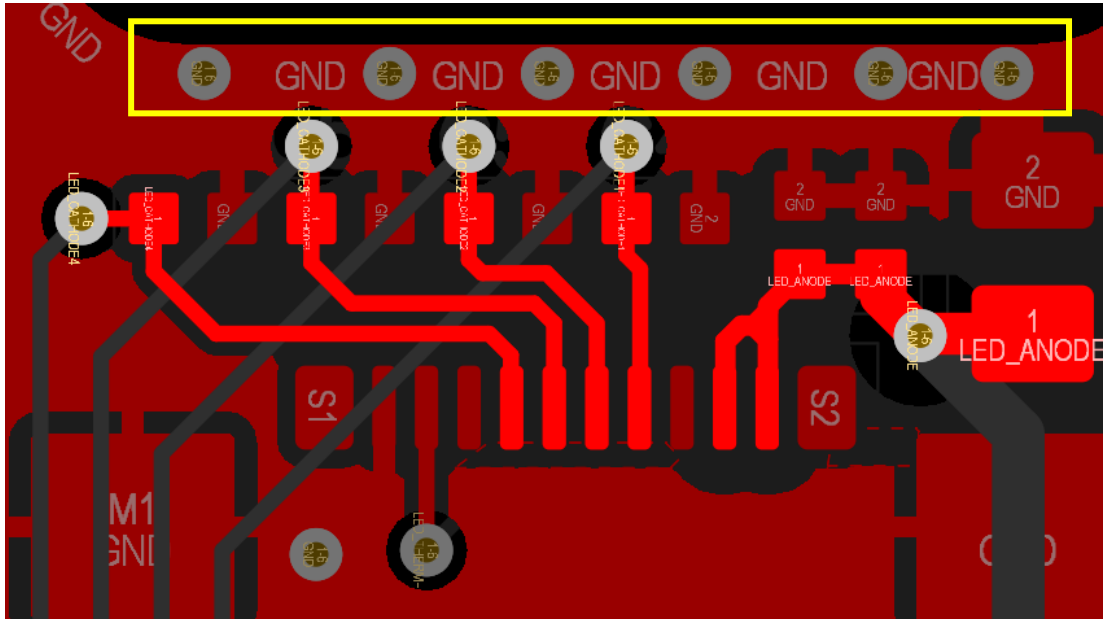

Design level (PCB Layout)(Cont.)

- PCB circuits and components are organized and segregated based on their functions, with **sensitive sensor circuits carefully grouped and positioned apart from power circuits** for optimal performance and interference prevention.

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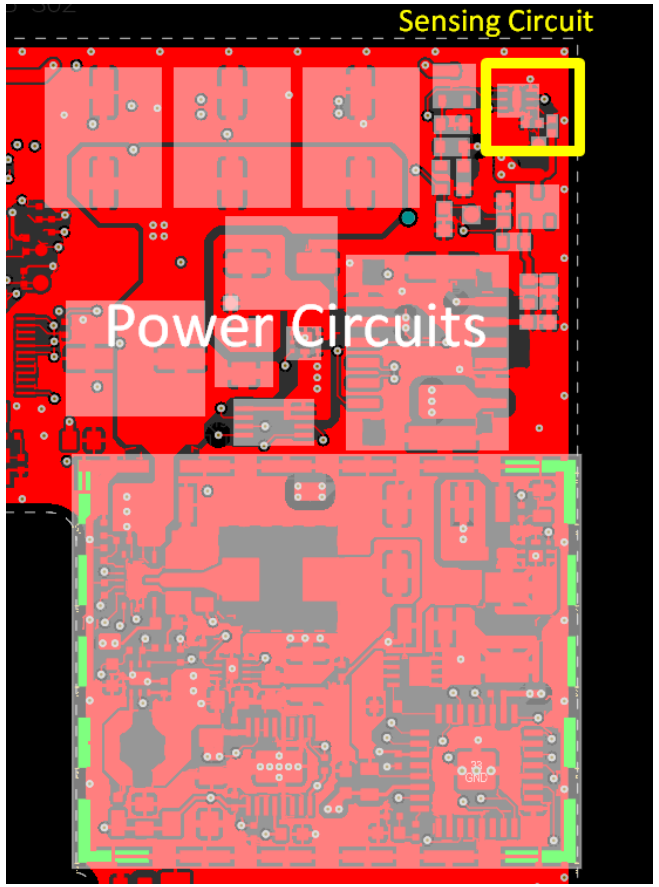

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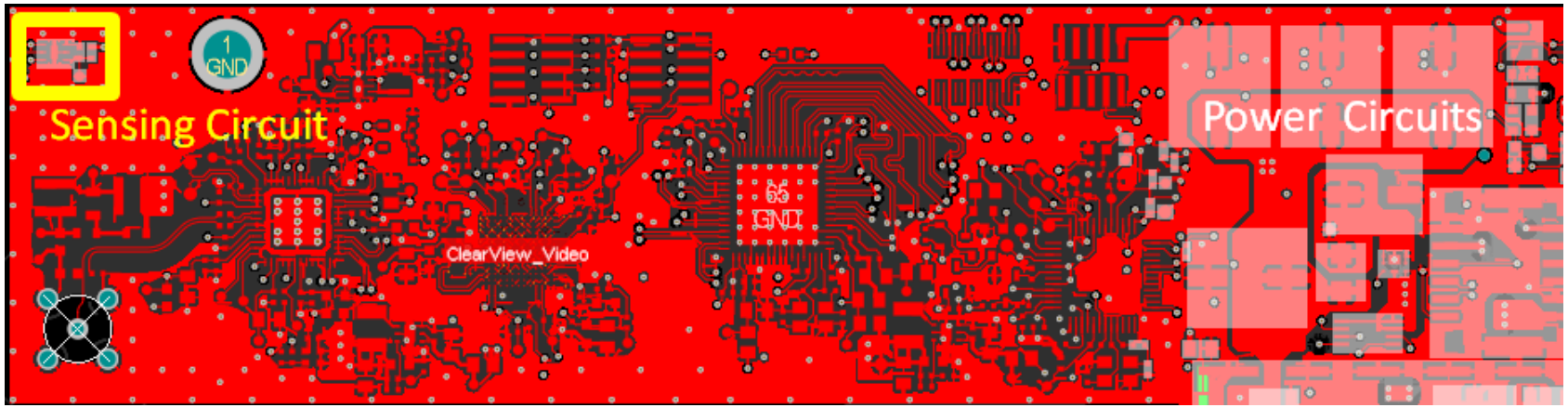
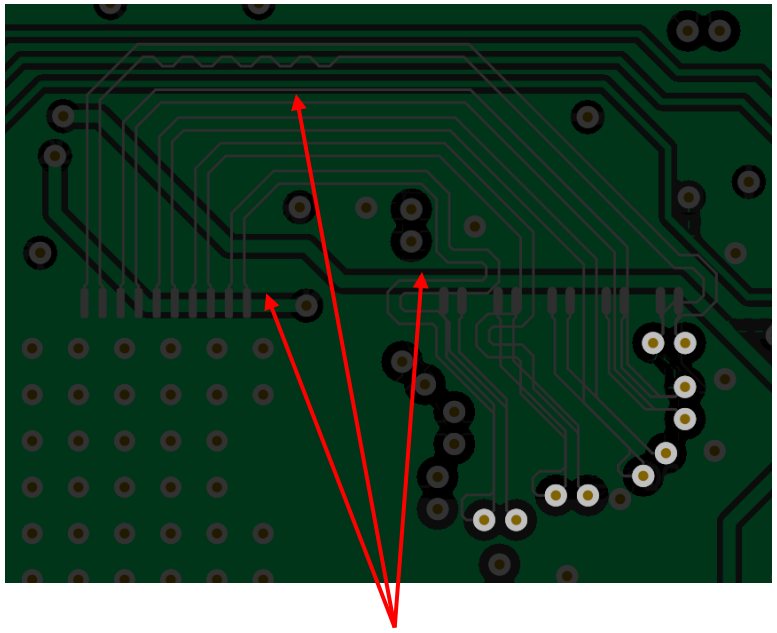


Design level (PCB Layout)(Cont.)

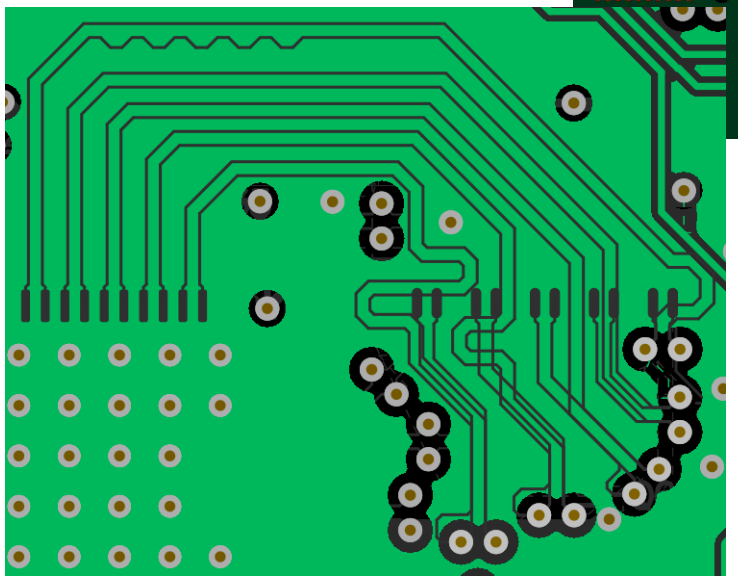
- Proper **GND references** were provided to optimize signal integrity, **minimize noise interference**, and maintain stable performance in **high-speed signals** and circuits.

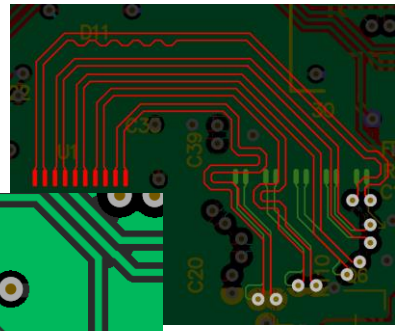
Before



Under high-speed signals, where power and other signals cross, GND references were not provided.

After

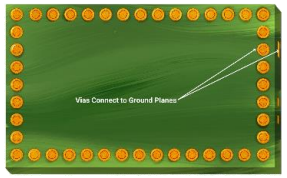




GND references were provided for routing and optimizing power and other signals under high-speed Signals.

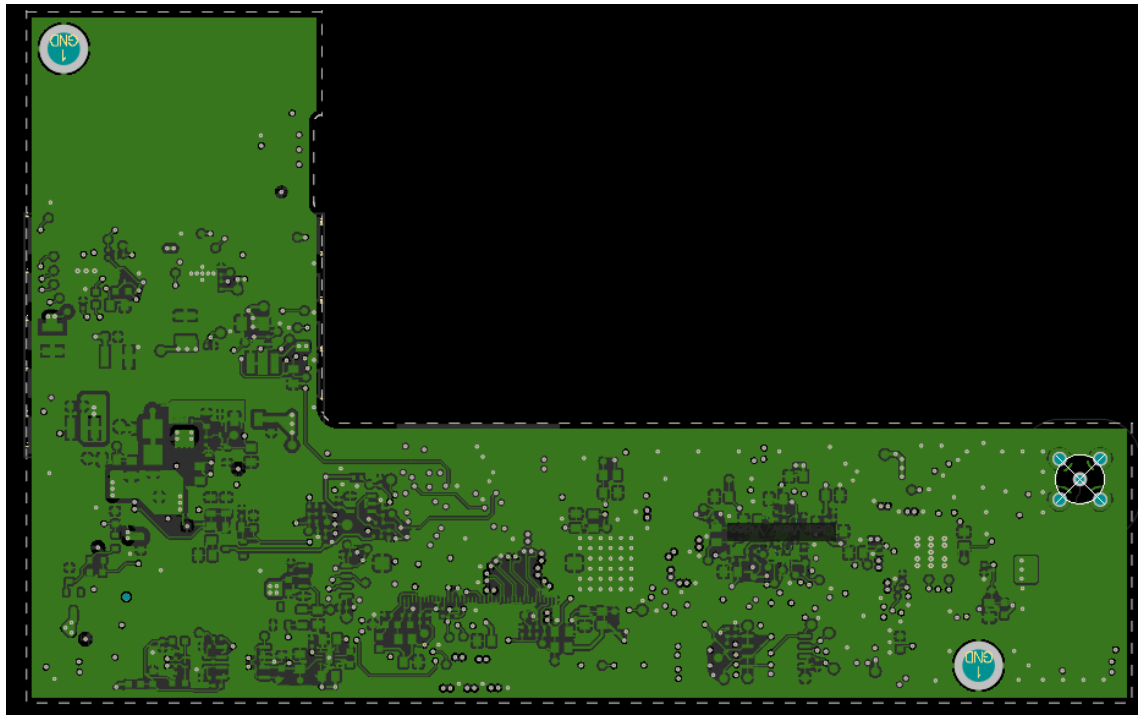
Design level (PCB Layout)

By **Stitching a ground vias on the PCB edge**, a Faraday cage is formed to confine signals within its boundary, effectively limiting emissions and interference.



Faraday's Cage

Before



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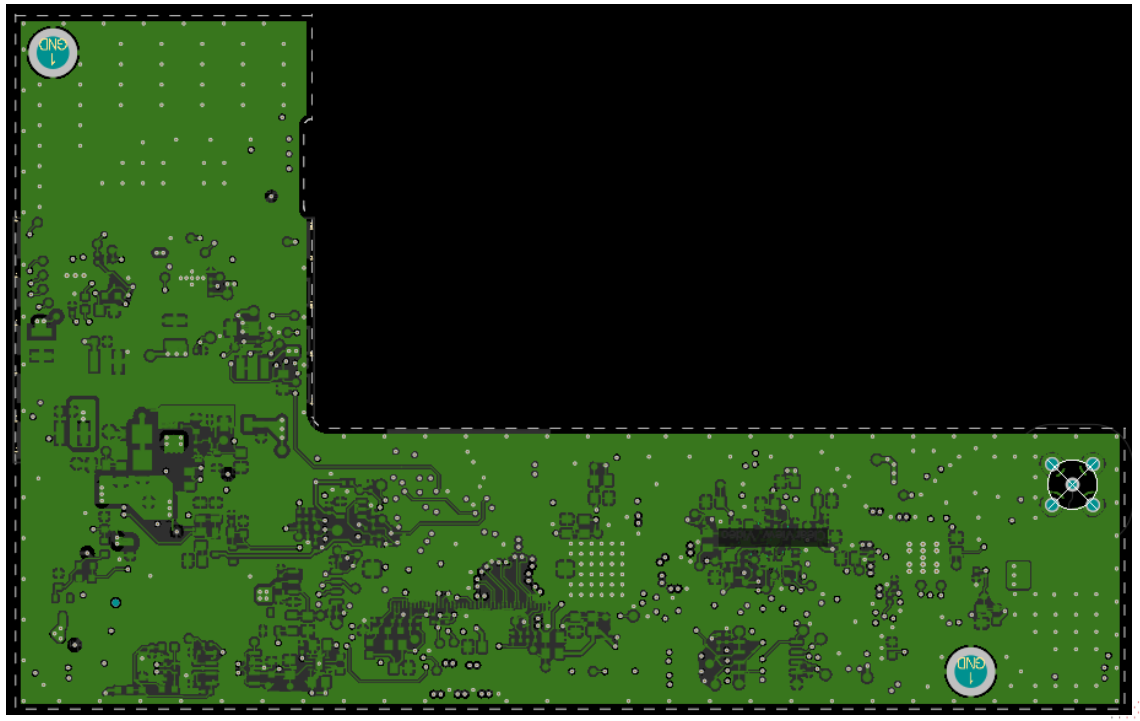
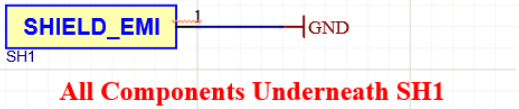
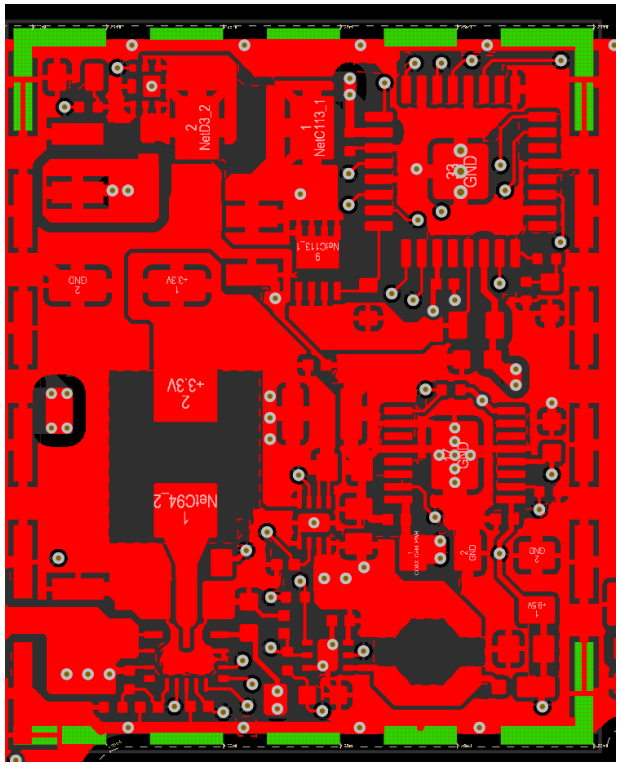
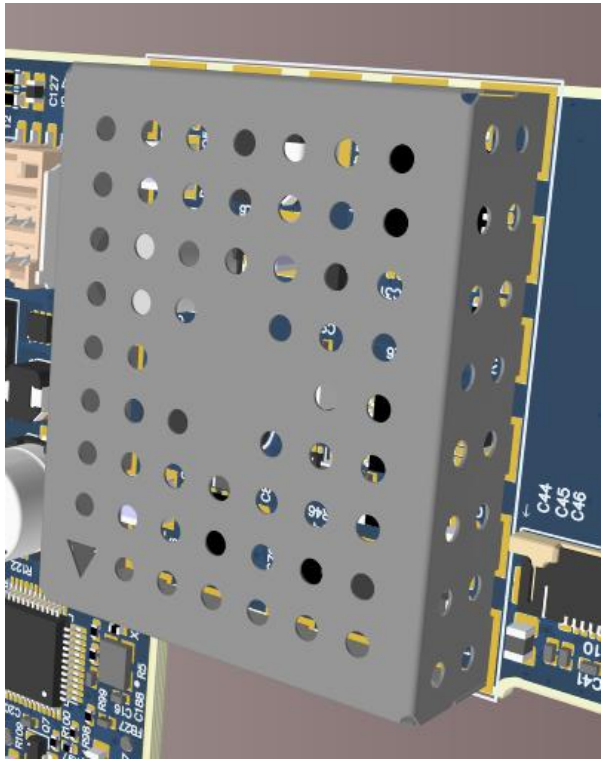


EMC shielding (Components level) (Cont.)



An **EMI shield** has been strategically introduced into the **power circuit section** to effectively **minimize electromagnetic interference (EMI),** ensuring cleaner signal transmission and enhanced circuit performance.





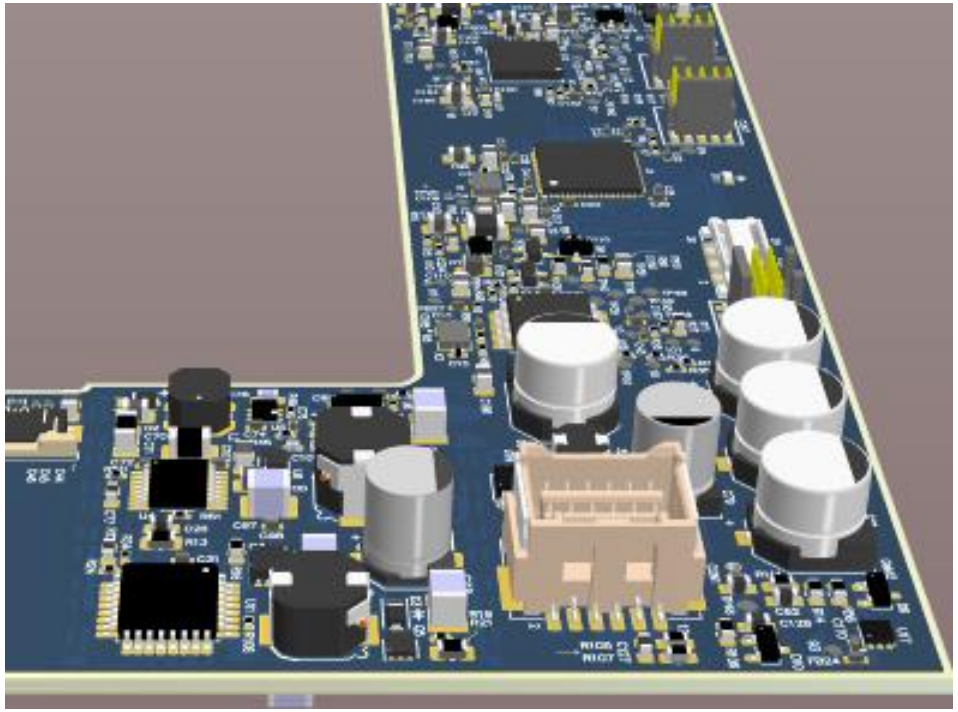
Circuits under the shield are,

3.3V Buck Regulator, Load switch (3.3V), 9.5V Boost Regulator, Low Noise Dual Camera Power Regulator and LED Driver.

EMC shielding (Components level)

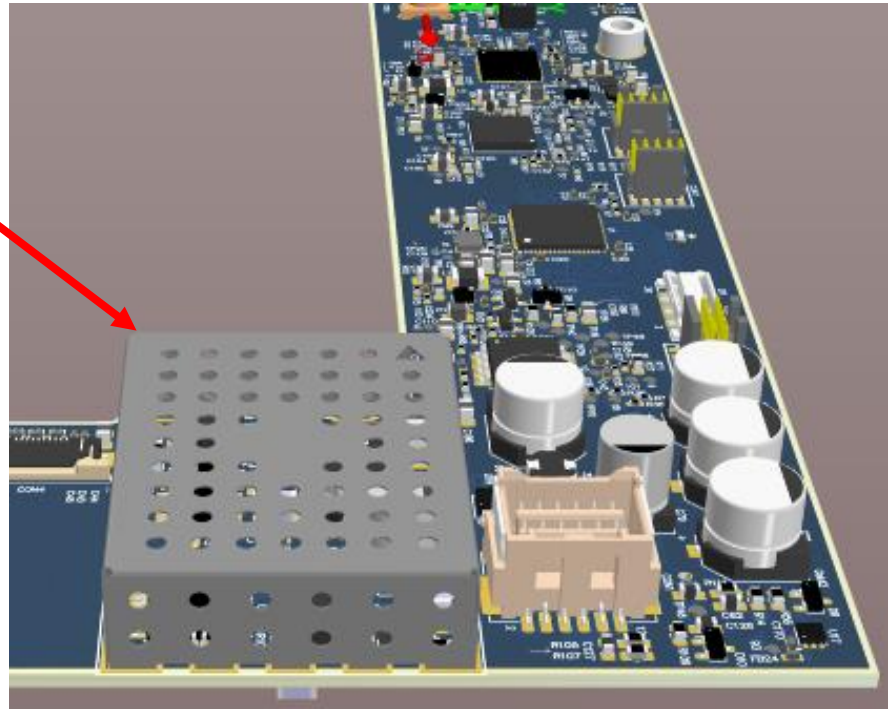
An ISO-27001 ISMS Certified Company

Before



EMI Shield

After



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A Global Engineering partner

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Client Testimonial

"We are delighted with the remarkable performance of this exceptional team. Despite challenges, they skillfully managed our circuit design, effectively addressing EMI/EMC concerns. Their design reflects a seamless integration of creativity and engineering expertise. What distinguishes them is their steadfast commitment to delivering cost-effective solutions while maintaining high-quality standards. In a remarkably short timeframe, they not only met but surpassed our expectations, achieving a significant project milestone. This team has proven to be the preferred choice for those in need of prompt, economical, and outstanding service ".

Conclusion

Our dedication to excellence and technical proficiency was evident in delivering customized solutions for EMI/EMC management that precisely met client requirements.

We excel in providing exceptional EMI/EMC management within PCB layouts, emphasizing cost reduction and showcasing our capability and reliability in consistently delivering outstanding outcomes. Our approach prioritizes quality and adherence to timelines.

Our partnership seamlessly combines expertise with personalized service, underpinned by technical proficiency to ensure exceptional results.