Design Optimization for EMI/EMC Compliance

Scope: EMI/EMC Mitigation

Application: Advanced Driver Assistance Systems

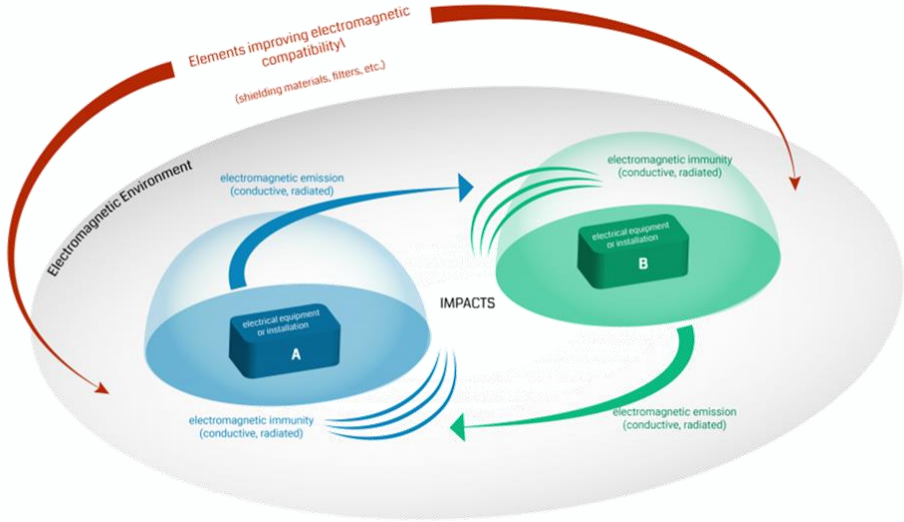
Image signals captured by vehicle-mounted cameras are crucial for Advanced Driver Assistance Systems (ADAS), enabling functions like lane departure warning, pedestrian detection, and traffic sign recognition. These signals provide essential visual data for detecting obstacles, monitoring blind spots, and maintaining safe distances from other vehicles. By analyzing these signals, ADAS systems enhance driving safety by alerting drivers to potential hazards and assisting in avoiding collisions.

EMI/EMC Compliance - Challenges

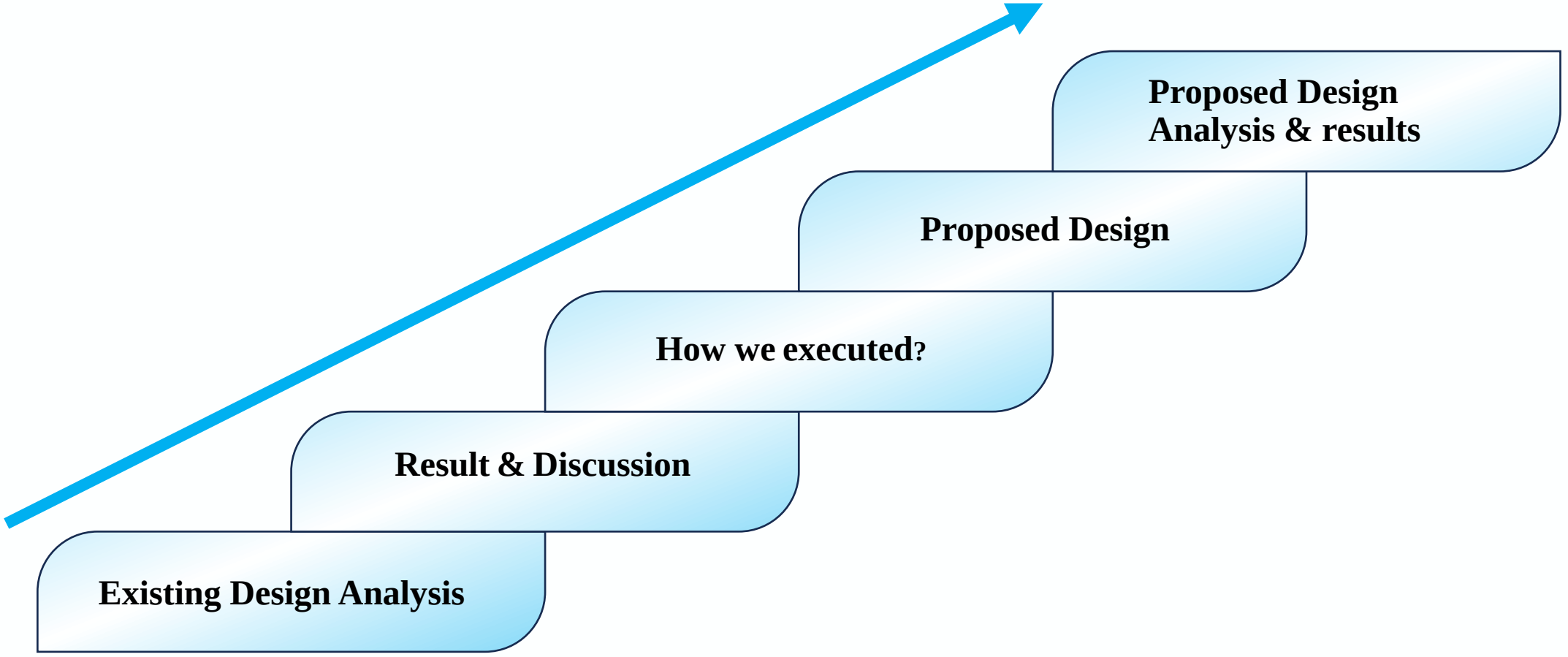
The client has come to us with a task of reducing the output noise caused by Electromagnetic Interference (EMI) and resolving Electromagnetic Compatibility (EMC) concerns on their PCB board.

Challenges:

- Minimizing output data noise for improved signal integrity.
- short timeline for project completion.
- Mitigating Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) issues on the board.
- High-level design changes are not preferred.
- Design changes do not impact the image signals group in the PCB design.
- The addition of major IC components to address this issue is not entertained.

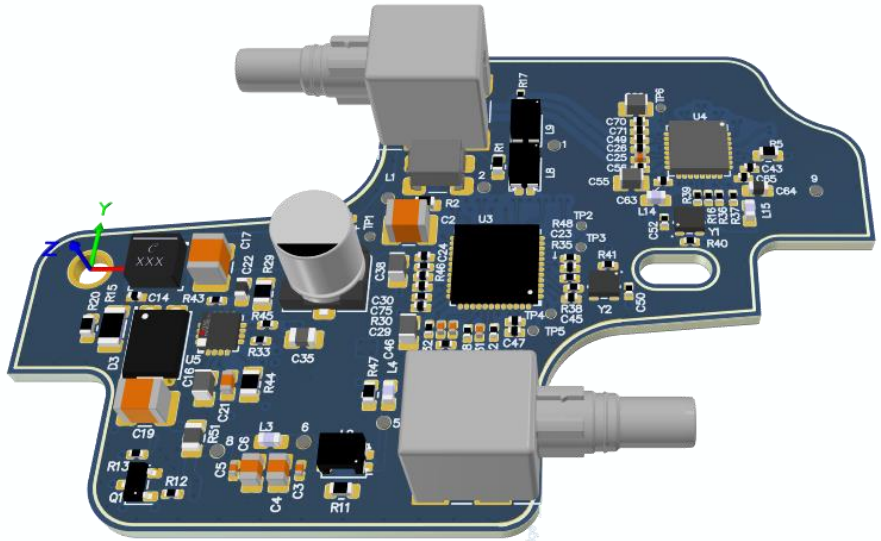


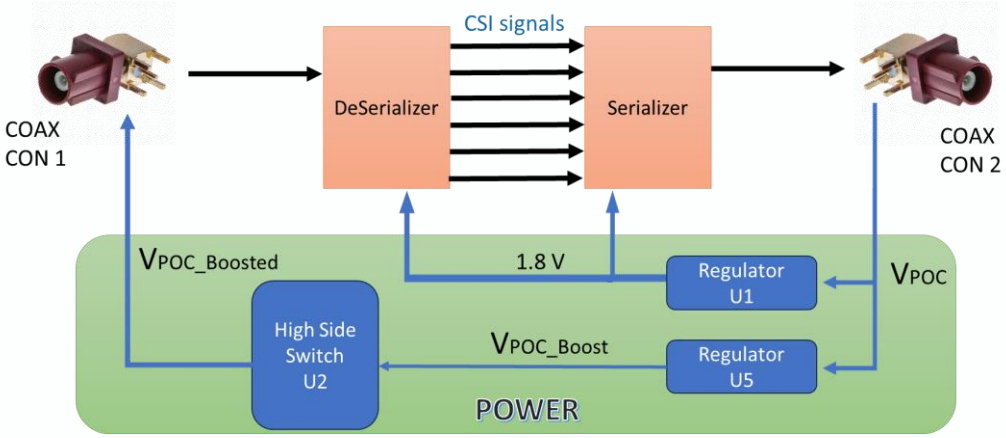
Hardware Design Optimization-SoW



Design Intent

- Image signals enter from coax connector 1, are deserialized, serialized, and sent to coax 2 for the intended purposes like image processing, data transmission, or signal communication within the ADAS system .
- Power is stepped down using regulator U1 from COAX connector 2 for the serializer and DeSerializer.
- Simultaneously, COAX power is converted using U5 and provided to the high-speed switch U2, transmitted through COAX connector 1.

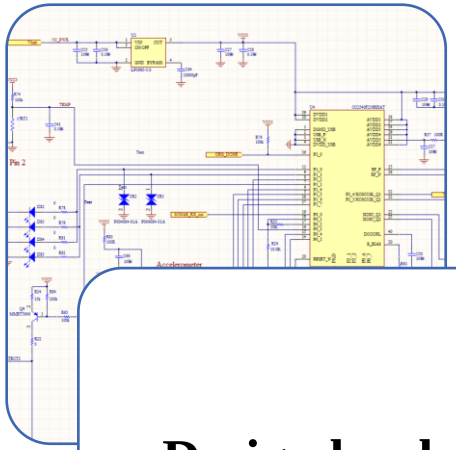




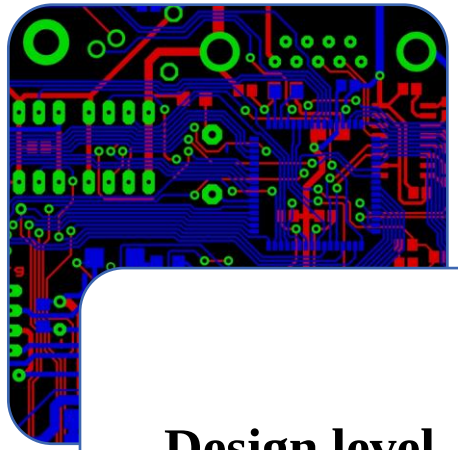
- The Design outputs shows unexpected peaks and drops in the output.
- The output is affected by a considerable amount of noise, which could potentially affect the performance and reliability of the system.

How we executed?

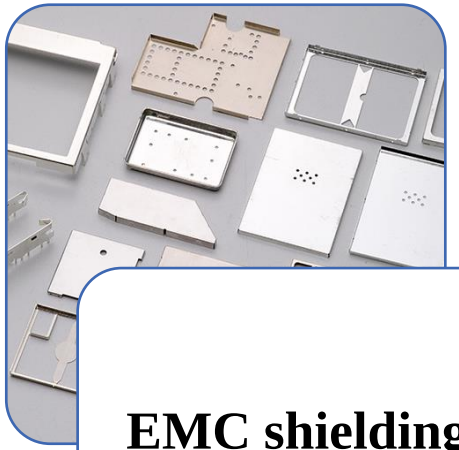
After reviewing the schematics and PCB of the existing project, the following design aspects have been identified at various levels to minimize unwanted noise at the monitoring points of the Regulator IC outputs.



Design level (Schematics)



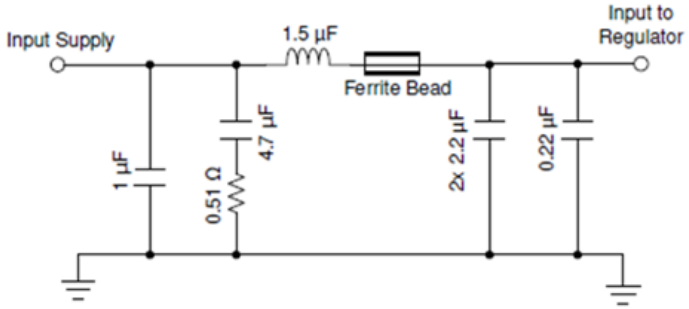
Design level (PCB Layout)



EMC shielding (Components level)

Design level (Schematics)

Adding the EMI filter before the Regulator Circuits (U1 & U5) in accordance with EMI guidelines significantly reduces noise at the entry level.

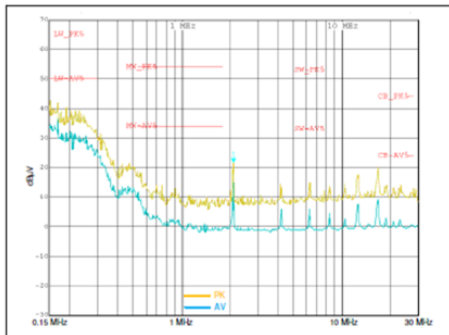


A. Input filter used only for EMI measurements shown in the *Section 9.2.5* section.

Figure 9-47. Typical Input EMI Filter

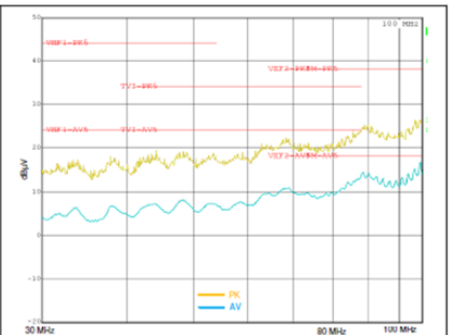
9.2.5 EMI Performance Curves

EMI results critically depend on PCB layout and test setup. The results given here are typical and given for information purposes only. Figure 9-45 shows the used EMI filter. The limit lines shown refer to CISPR25 class 5.



LM63625DQ I_{OUT} = 2.5 A | V_{OUT} = 5 V Dither | f_{SW} = 2100 kHz

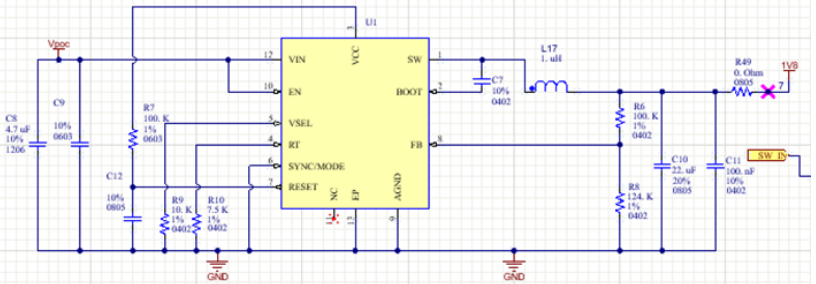
Figure 9-45. Typical Conducted EMI 0.15 MHz to 30 MHz



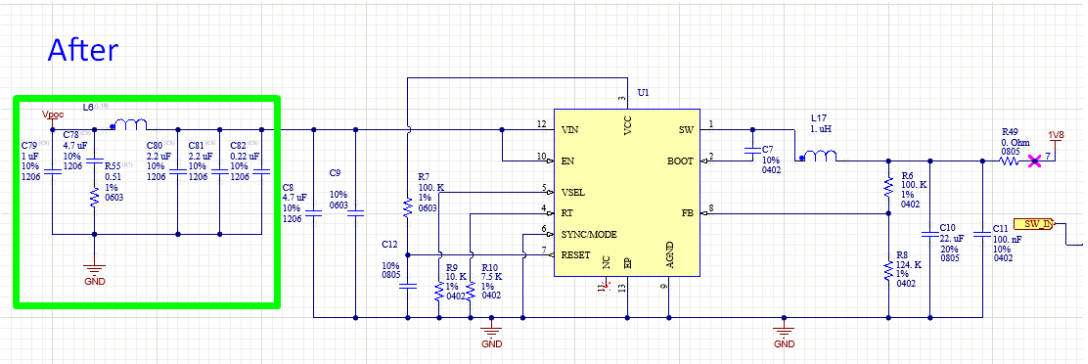
LM63625DQ I_{OUT} = 2.5 A | V_{OUT} = 5 V Dither | f_{SW} = 2100 kHz

Figure 9-46. Typical Conducted EMI 30 MHz to 108 MHz

Before

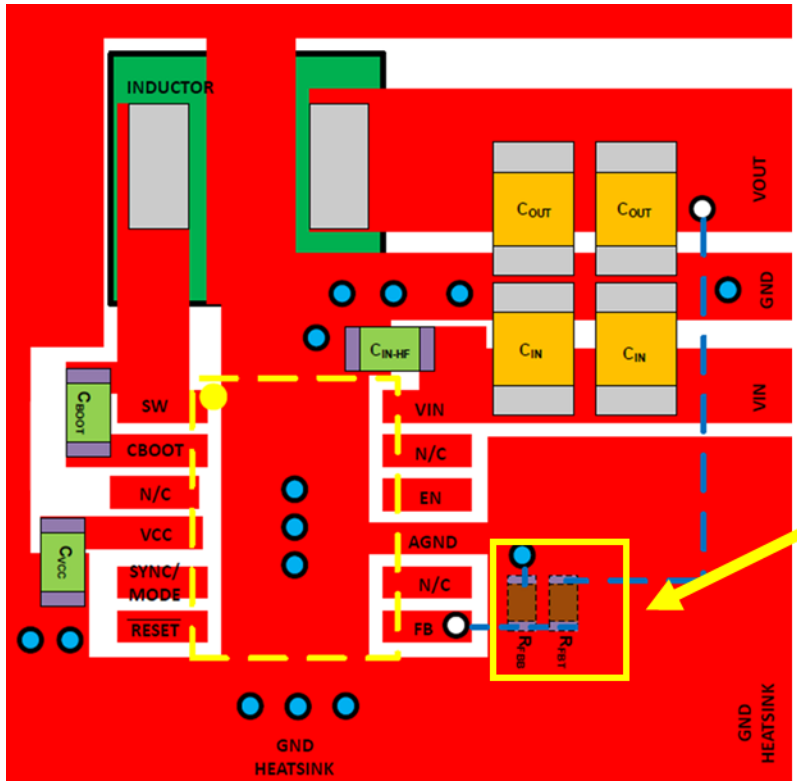


After



Design level (PCB Layout)(Cont.)

1. In the layout, placement, and routing, **implementation for the FB pin of ICs (U1 & U5)** was executed according to layout recommendations, ensuring optimal performance and functionality.



Protect Sensitive Nodes

Protecting sensitive nodes is also very important for SMPS layout. One such node is the feedback (FB) pin. The FB node is a high impedance node. Avoid placing the resistor divider far away from the FB node and connecting FB node with long traces, as shown in Figure 15. To minimize the parasitic capacitance and noise pickup by the trace to FB node, the FB trace should be short and thin. As shown in Figure 16, it is recommended to place the resistor divider as close as possible to the FB pin and route a thin trace from output voltage sense away from noisy path, preferably from the other side of a shielding plane.

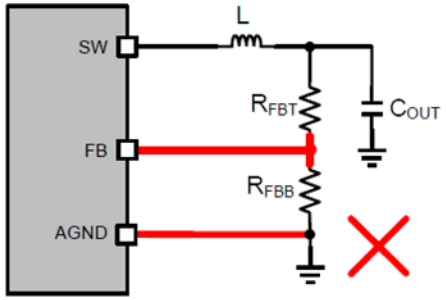


Figure 15. Avoid Long Traces to the FB Node

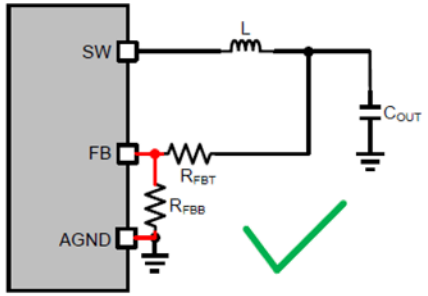
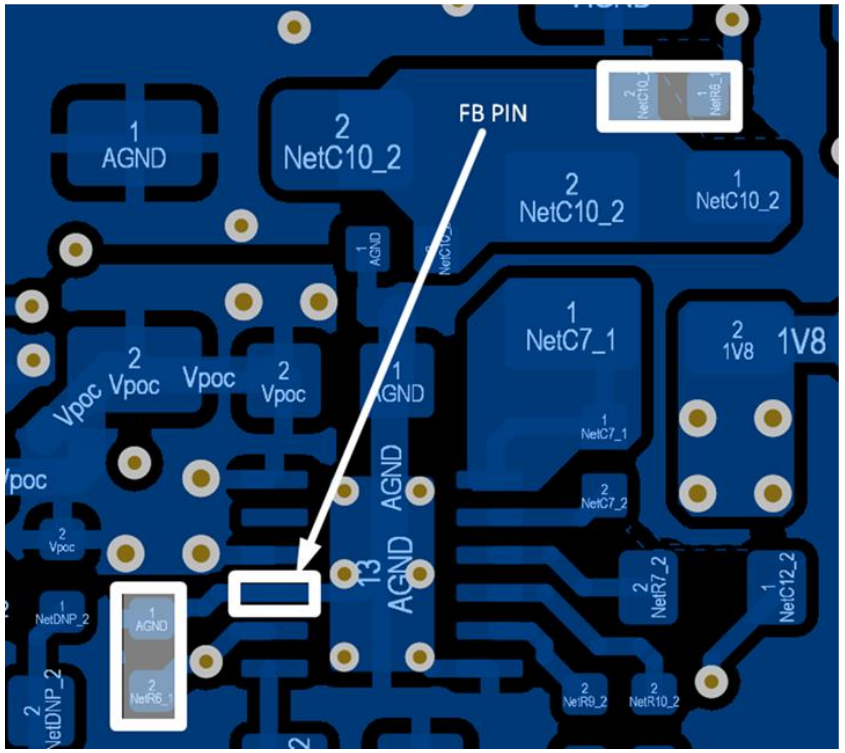


Figure 16. Use Short and Thin Traces at the FB Node

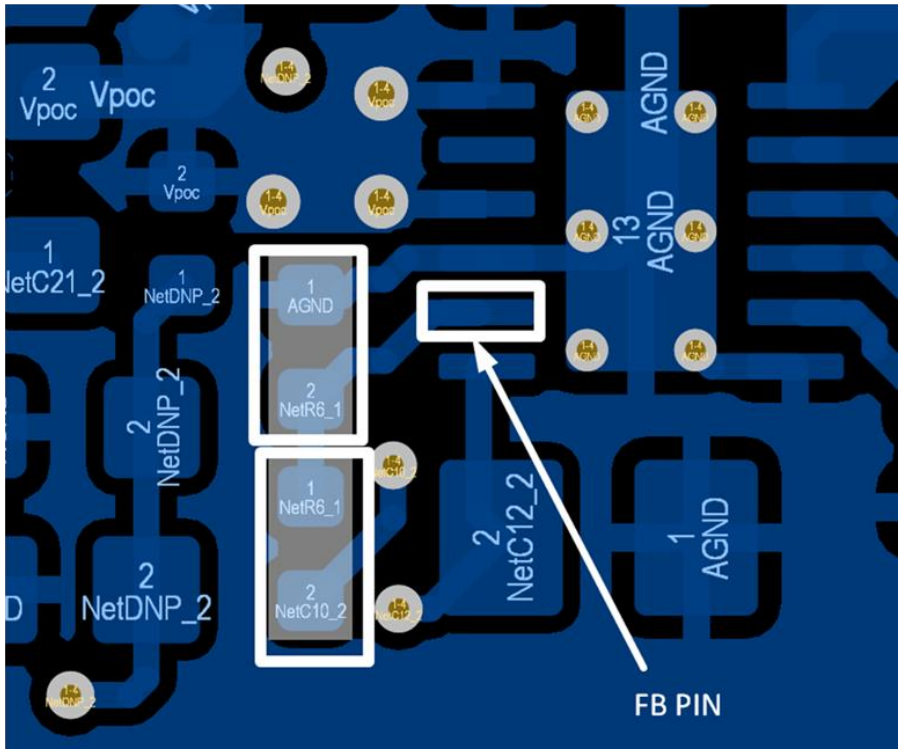
Design level (PCB Layout)(Cont.)

- Implemented for resistor divider circuit for the FB pin of regulator **IC (U1)**

Before



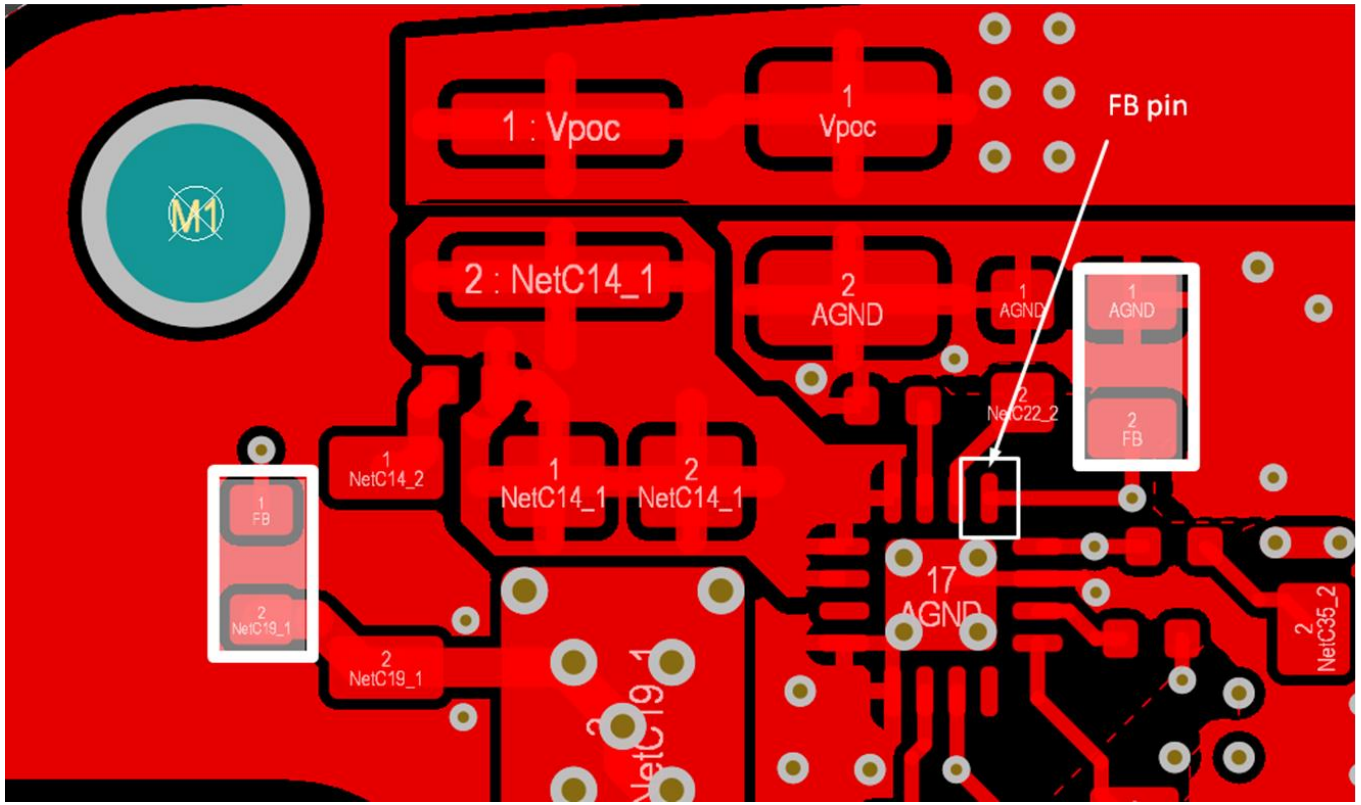
After



Design level (PCB Layout)(Cont.)

- Implemented for resistor divider circuit for the FB pin of regulator **IC (U5)**

Before



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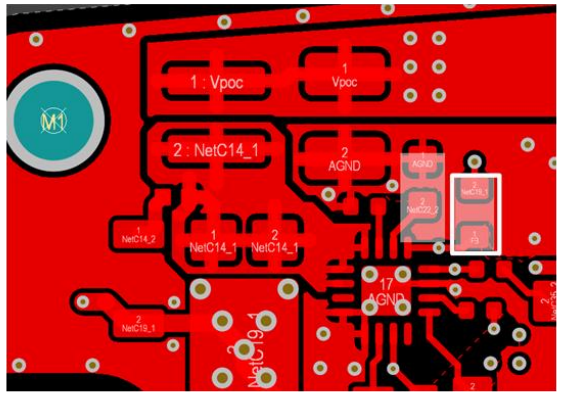
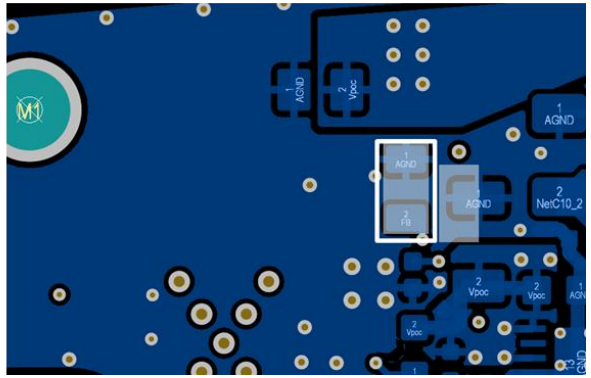




Design level (PCB Layout)(Cont.)

2. Following guidelines, placement and routing were optimized to provide a **ground plane at the switch nodes of the regulator ICs** on this 4-layer board.

2.4 *Ground Shielding*

Better EMI results can be achieved by adding an unbroken ground plane as a middle layer in the PCB. If the IC is placed on the top layer and the high di/dt paths are routed on the top layer, the ground plane at the midlayer allows a mirror return current to be formed right underneath a top layer current. The mirror current path minimizes the current loop area and the magnetic field generated by the two opposite direction currents will be almost canceled.

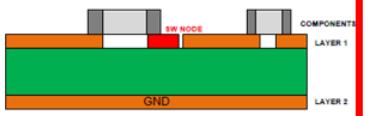


Figure 9. Cross Section Illustration of the Two Layer Board

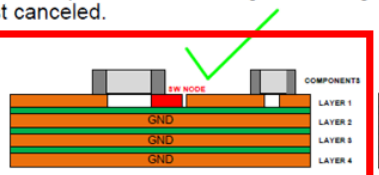


Figure 10. Cross Section Illustration of the Four Layer Board with Unbroken Ground Planes

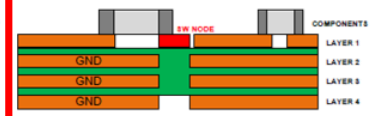


Figure 11. Cross Section Illustration of the Four Layer Board with Broken Ground Planes

Figure 12. Radiated EMI Result from the Two Layer Board

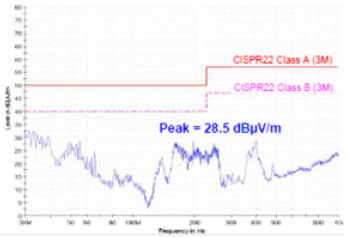


Figure 13. Radiated EMI Result from the Four Layer Board with Unbroken Ground Planes

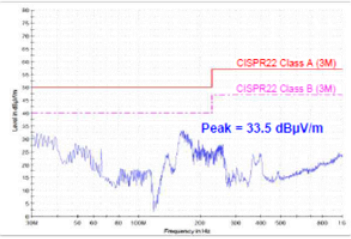


Figure 14. Radiated EMI Result from the Four Layer Board with Broken Ground Planes

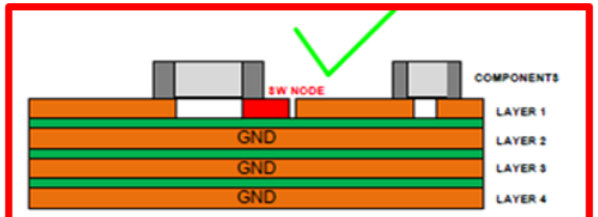


Figure 10. Cross Section Illustration of the Four Layer Board with Unbroken Ground Planes

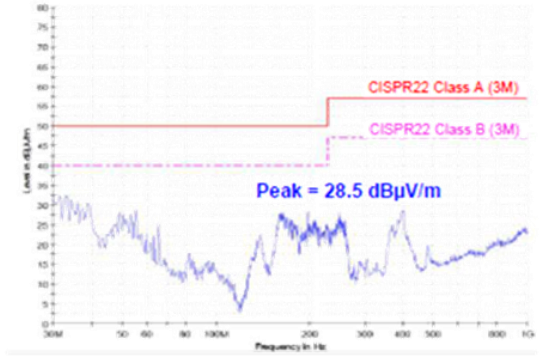
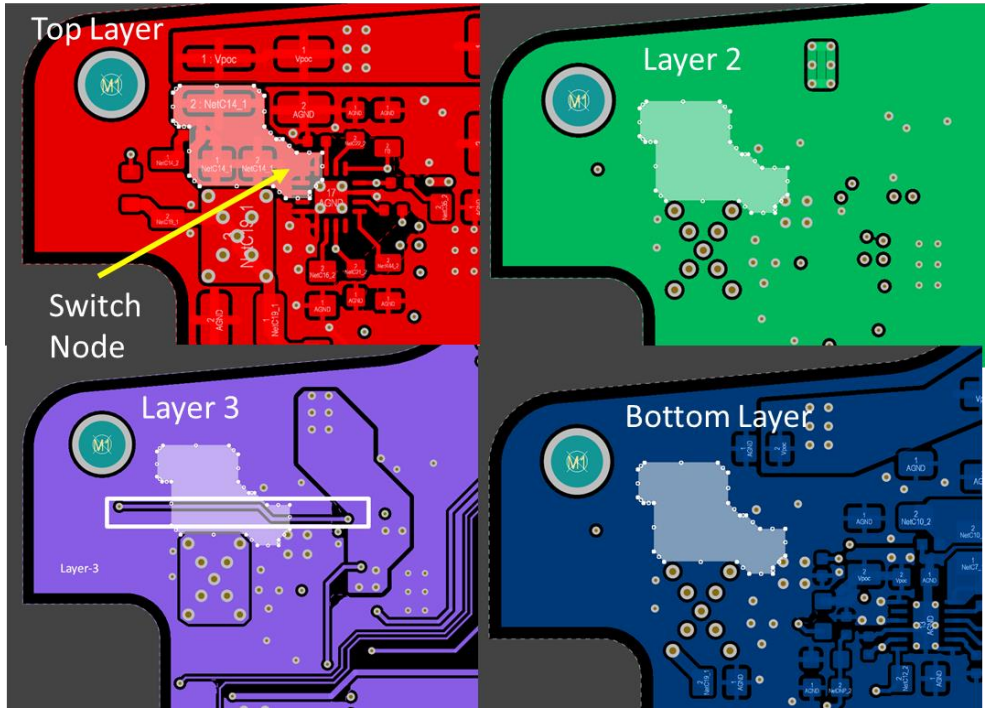


Figure 13. Radiated EMI Result from the Four Layer Board with Unbroken Ground Planes

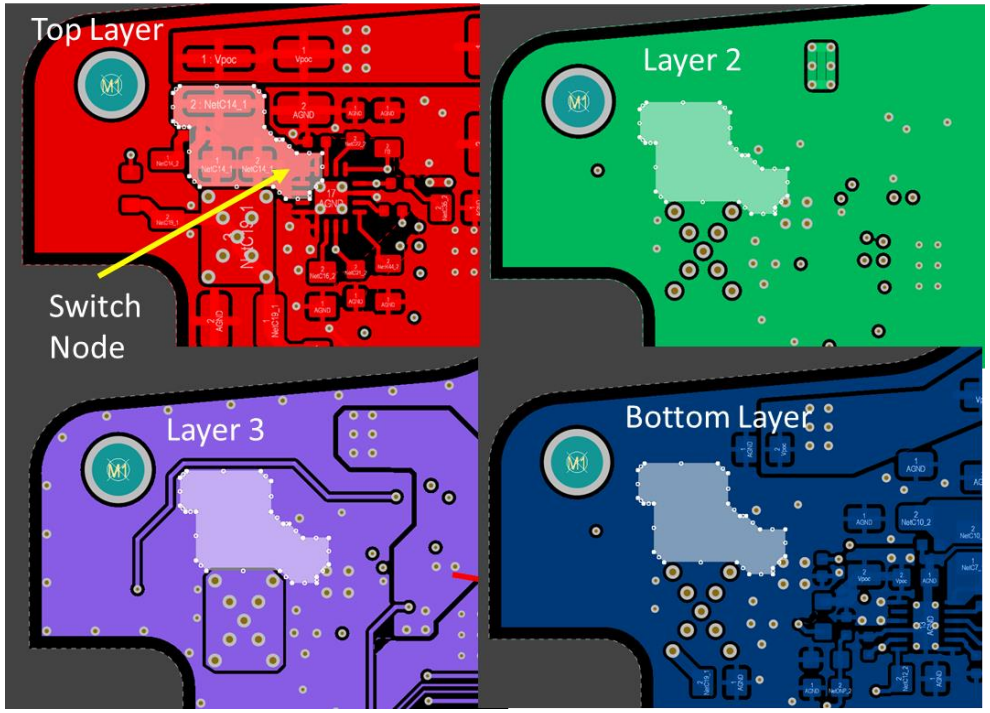
Design level (PCB Layout)(Cont.)

- Implemented for **ground plane at the switch nodes of the regulator IC (U5)**

Before



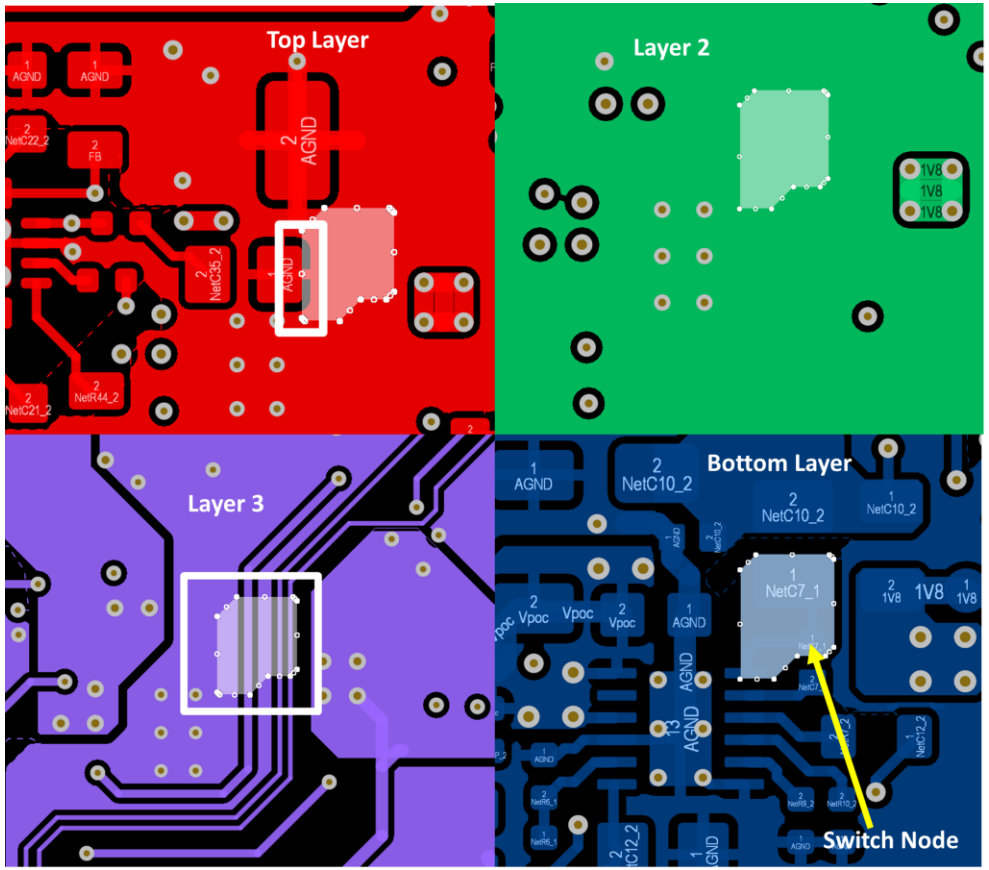
After



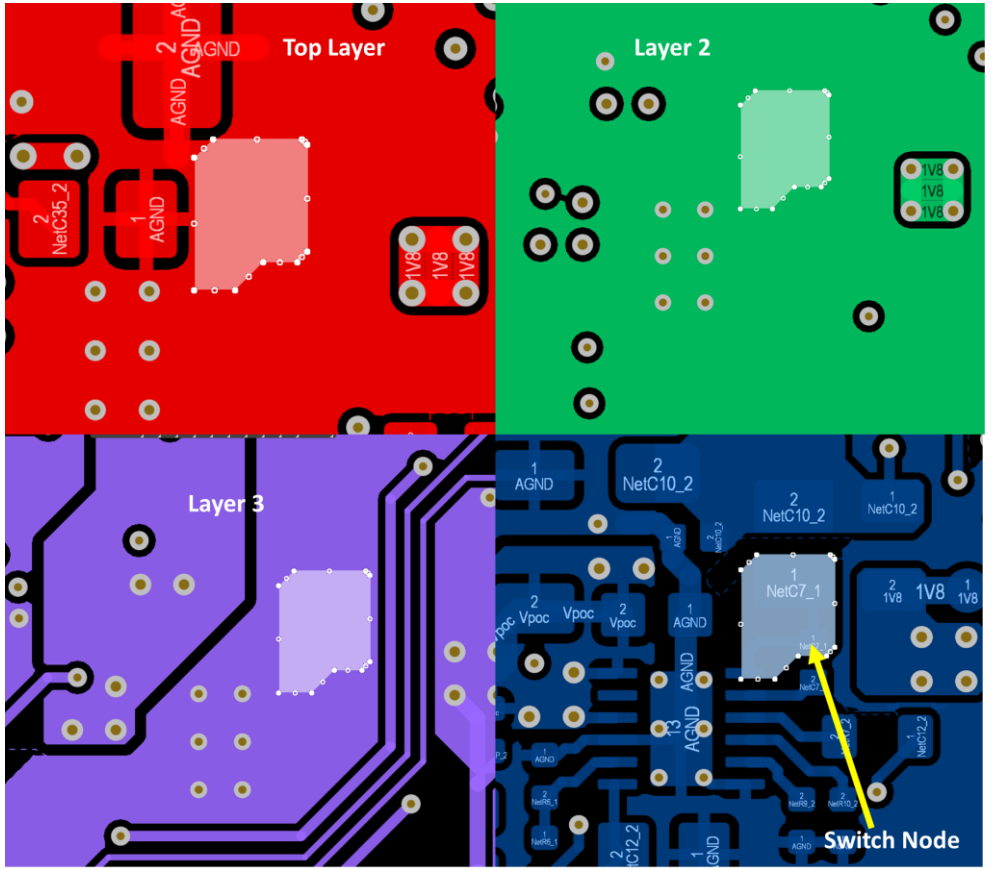
Design level (PCB Layout)(Cont.)

- Implemented **for ground plane at the switch nodes of the regulator IC (U1)**

Before



After

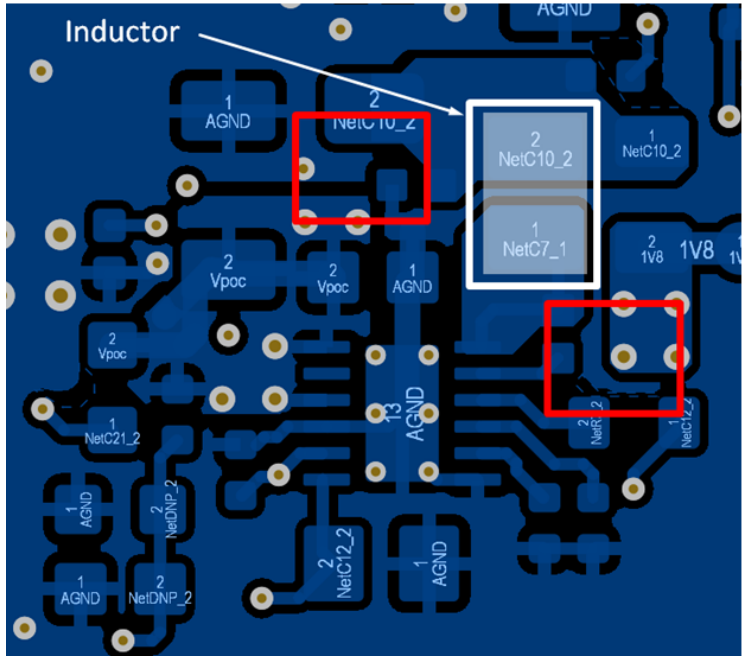


Design level (PCB Layout)(Cont.)

3. The **copper under the switching inductor was removed** as a guideline principle for component placement. This was done to mitigate EMI issues and interruptions in the switching process.

4. The hanging copper near the Regulator ICs was removed, and the input and output filter capacitors' ground connections were connected to the device ground, following the regulator datasheet.

Before



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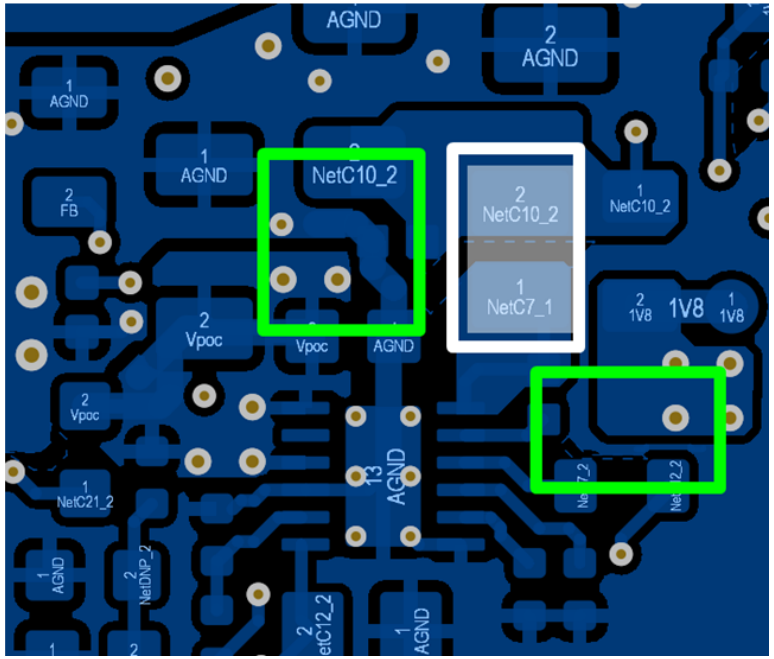
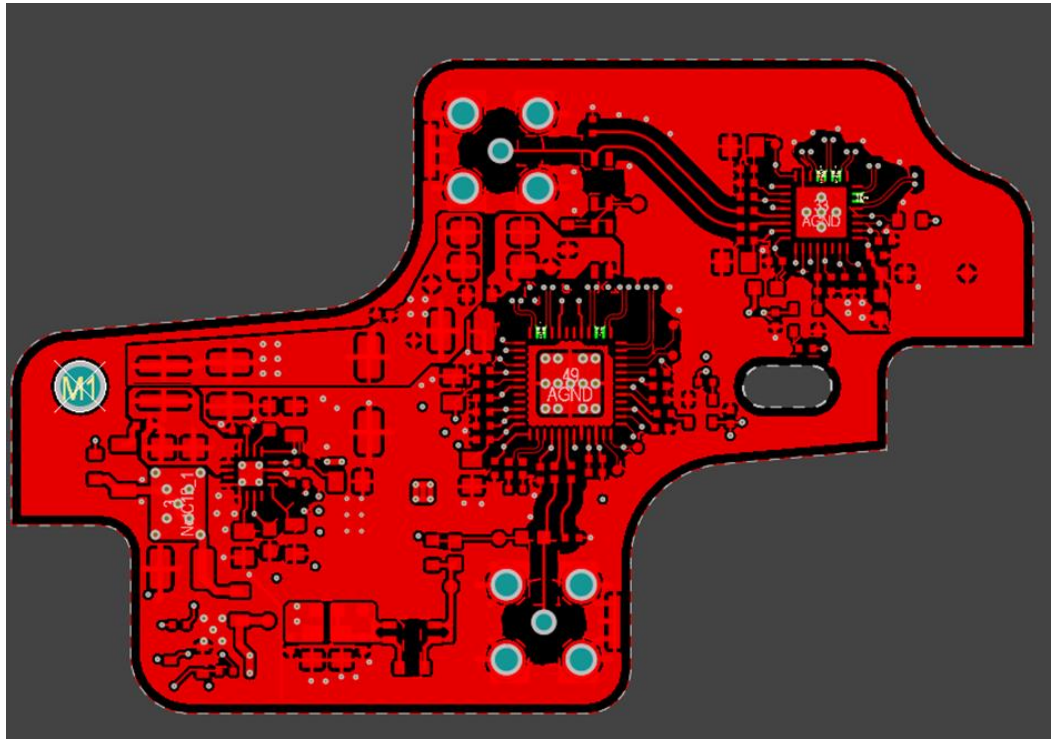


Design level (PCB Layout)(Cont.)

5. **GND vias are stitched** along the PCB perimeter to ensure effective grounding and minimize electromagnetic interference, enhancing overall performance and reliability.

Before



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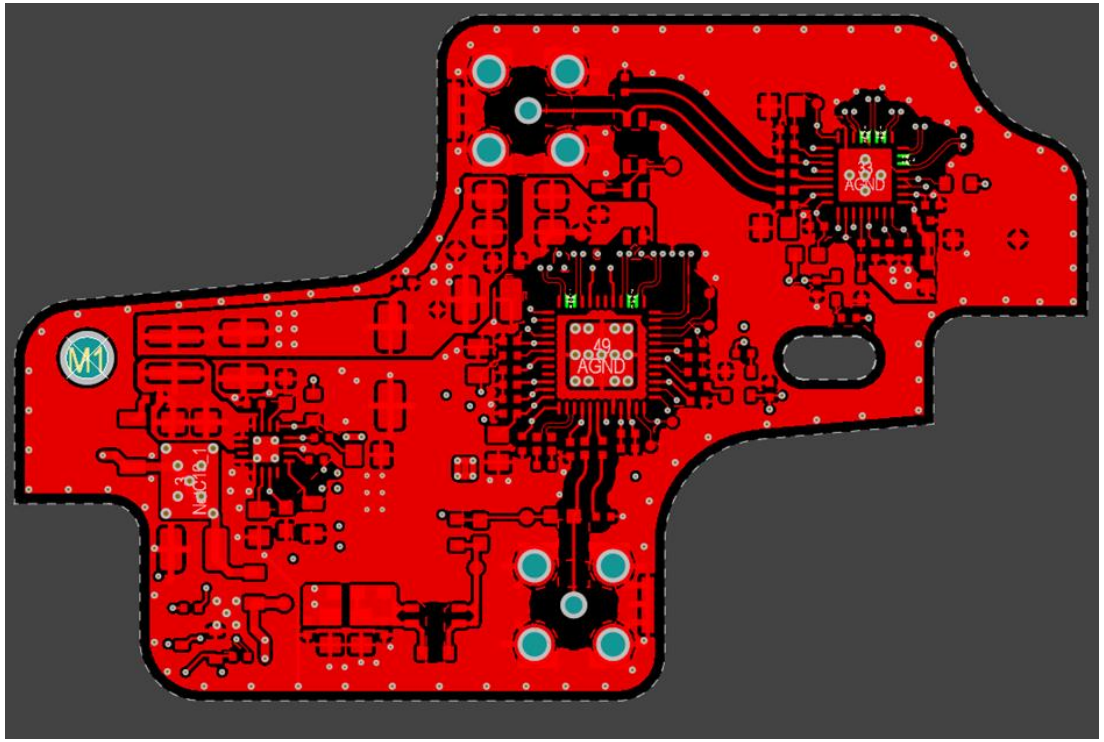
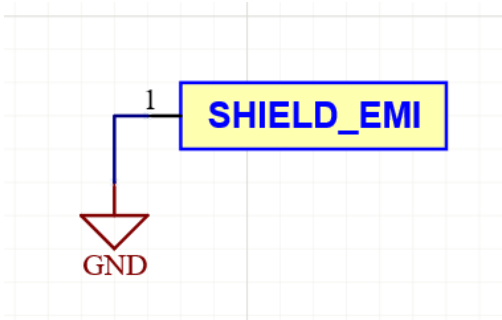


EMC shielding (Components level)

(After implementing design-level methods, if additional noise reduction is necessary, consider incorporating the mentioned features.)
Consider using upcoming power boards while also incorporating the mentioned features.

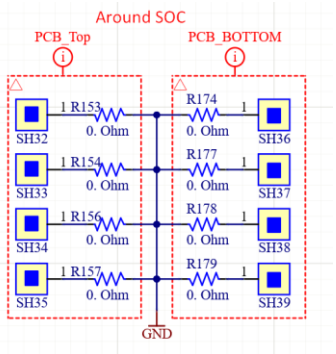


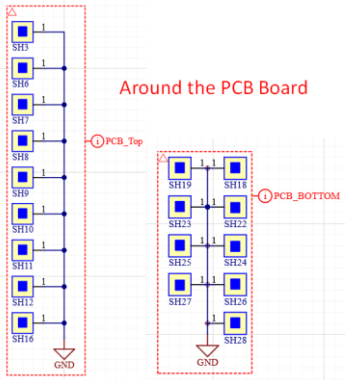
Suggestion:

- Implementing(EMI/EMC shields or gaskets around EMC-sensitive components, as illustrated in the provided images

- Consider placing **spring clips or fingers** around both the top and bottom layers of the PCB board.

Spring clips





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Client Testimonial

"We're thrilled with the exceptional performance of this outstanding team. Despite facing challenges, they adeptly managed our circuit design, successfully addressing EMI/EMC concerns. Their design showcases a flawless blend of creativity and engineering proficiency. What sets them apart is their unwavering dedication to delivering cost-effective solutions while upholding high quality standards. In a remarkably short time, they not only met but exceeded our expectations, reaching a significant project milestone. This team has proven to be the top choice for those seeking prompt, affordable, and excellent service."

Conclusion

Our commitment to excellence and technical expertise was evident in the successful delivery of tailored EMI/EMC handling solutions that met the client's requirements.

Our commitment shines through in delivering exceptional EMI/EMC handling in PCB layouts, not only reducing costs but also demonstrating our capability and reliability in consistently delivering outstanding results. Our approach prioritizes quality and strict adherence to timelines.

Our partnership seamlessly integrates expertise with personalized service, complemented by technical proficiency.