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Optimized Hardware Design-EMI/EMC Compliance

Scope: Hardware Design-EMI/EMC Mitigation

Application: Battery Management System

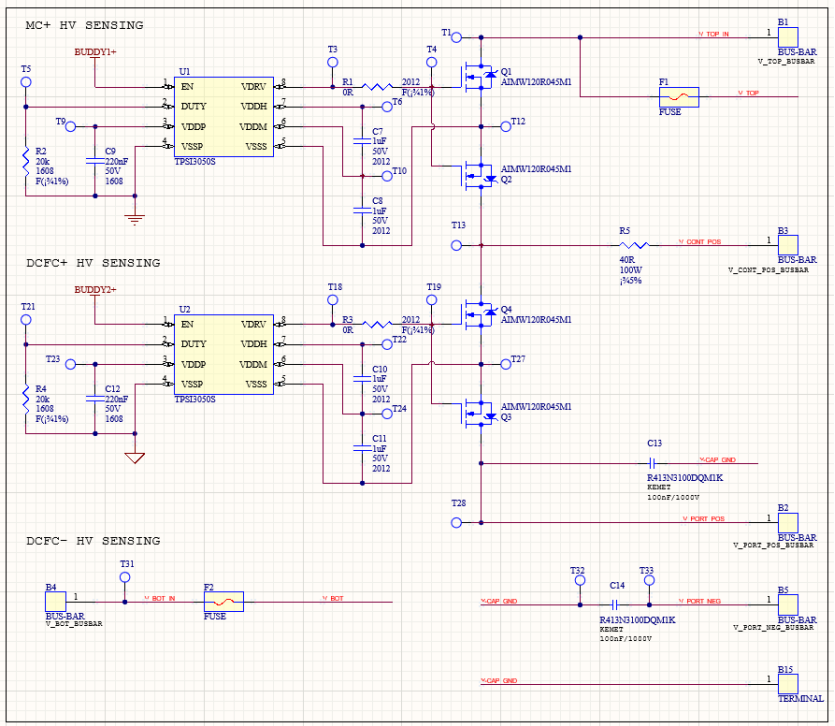
The efficient management of rechargeable batteries is intricately connected to the critical hardware circuit design of a Battery Management System (BMS), commonly recognized as the central intelligence of electric vehicles. Our particular focus is on the optimization of the PCB board, specifically the pre-charging circuit, to address and mitigate potential EMI/EMC issues for enhanced overall performance..

Challenges

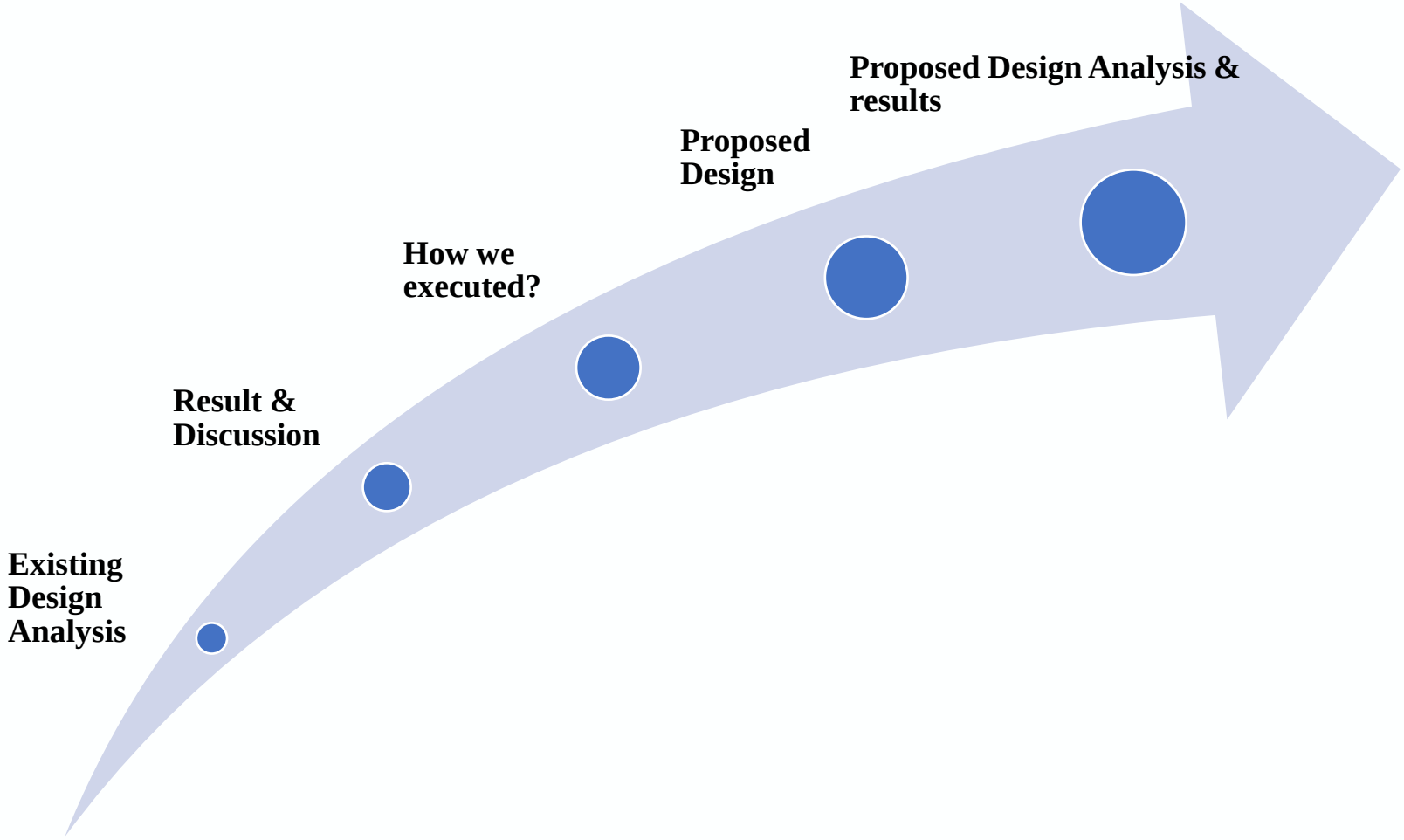
The client has approached us with the challenge of minimizing output noise caused by Electromagnetic Interference (EMI) and addressing Electromagnetic Compatibility (EMC) issues on their PCB board.

Challenges:

- Achieving a target output voltage of **10V** with a tolerance of +/- 10% in the given design.
- Minimizing output data noise for improved signal integrity.
- short timeline for project completion.
- Mitigating Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) issues on the board.



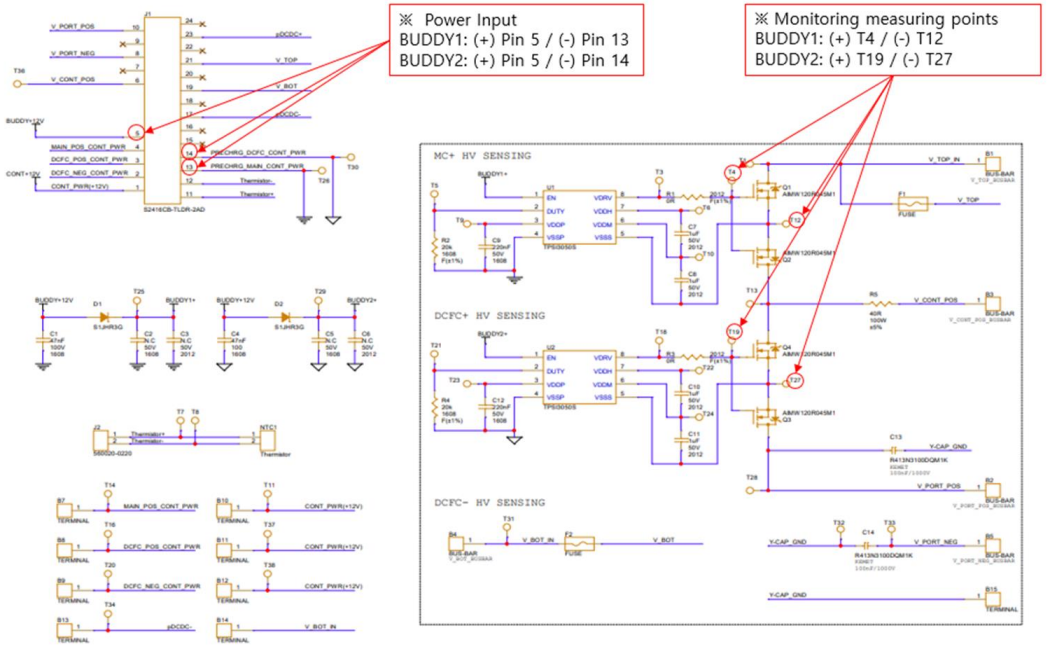
Hardware Design Optimization-SoW

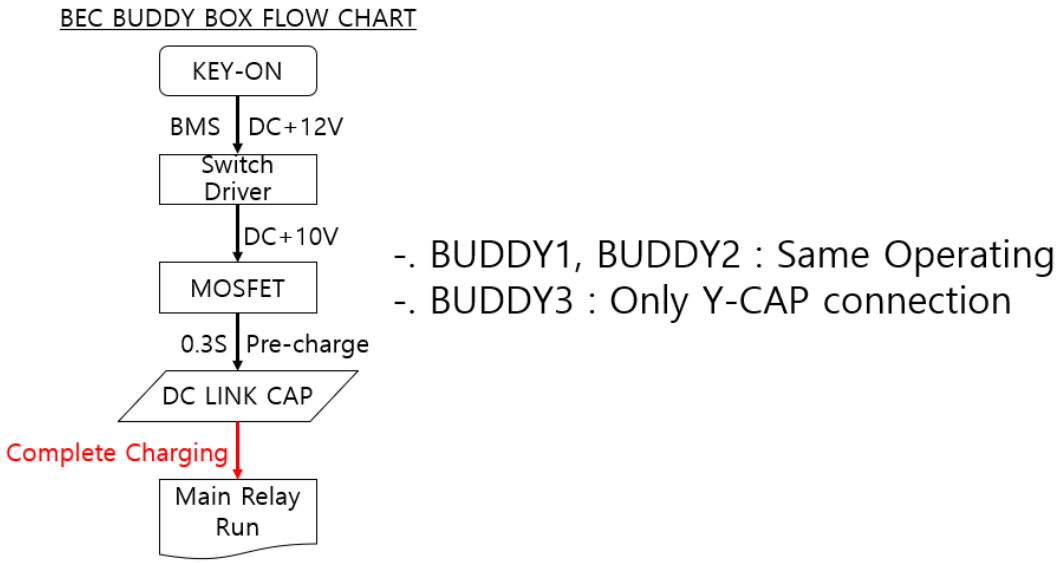


Design Intent

Design :Pre-Charging circuit

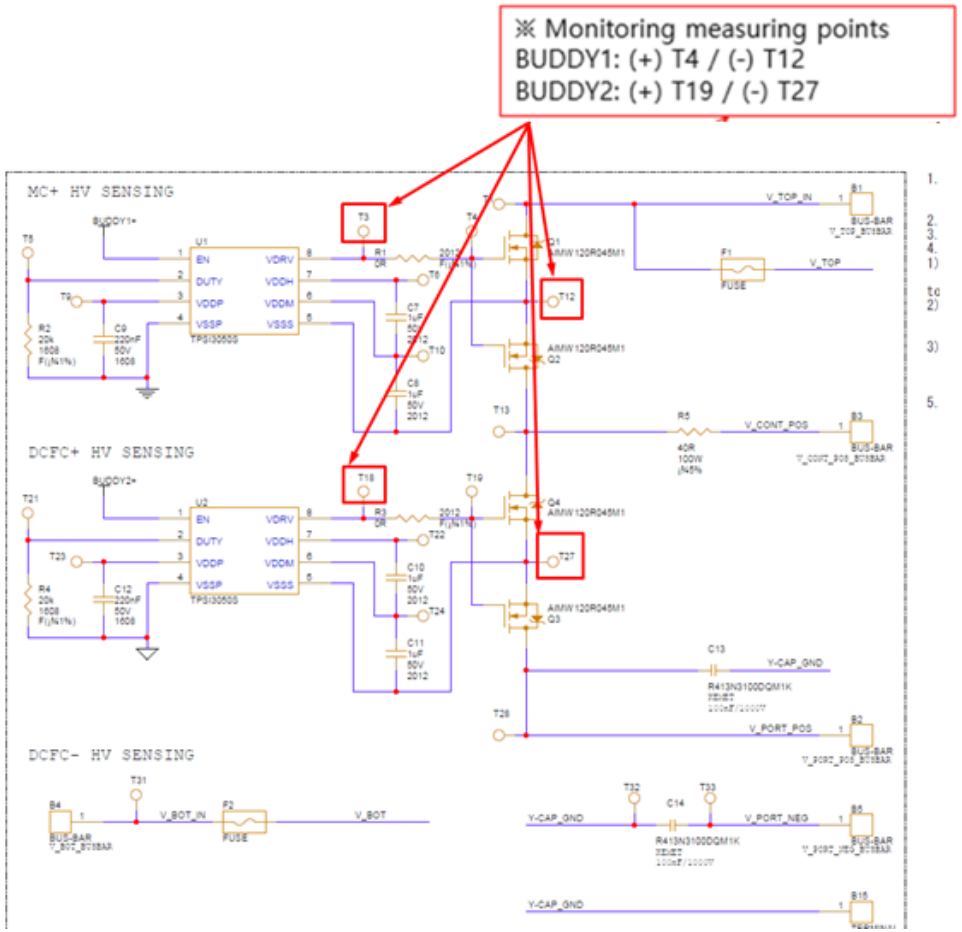
This circuit serves as a pre-charging design with the critical requirement of providing a DC output of +10V for the switch driver. This +10V supply is essential for initiating the turning on of the MOSFETs, which in turn activates the DC link capacitor for a pre-charging duration of 3 seconds. Upon completion of the pre-charging process, the main relay is then activated.



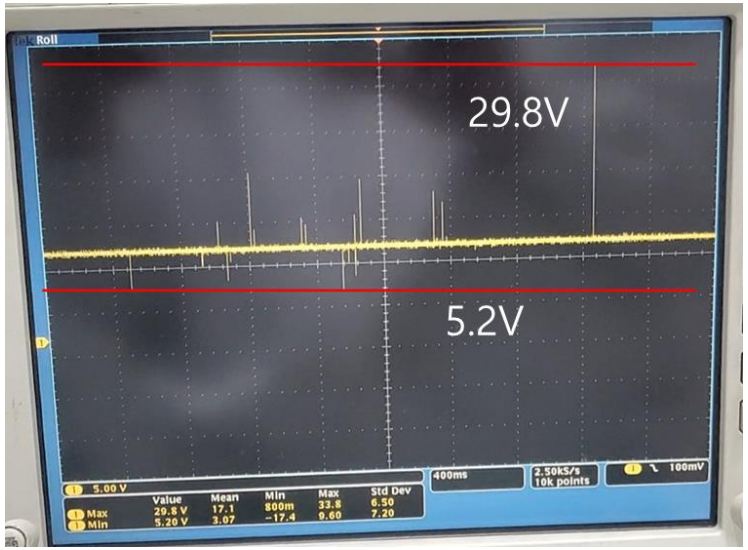


-. BUDDY1, BUDDY2 : Same Operating
-. BUDDY3 : Only Y-CAP connection

Existing Design Analysis



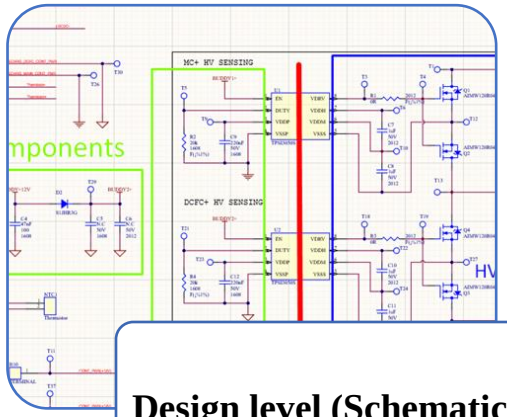
Existing Design Analysis output



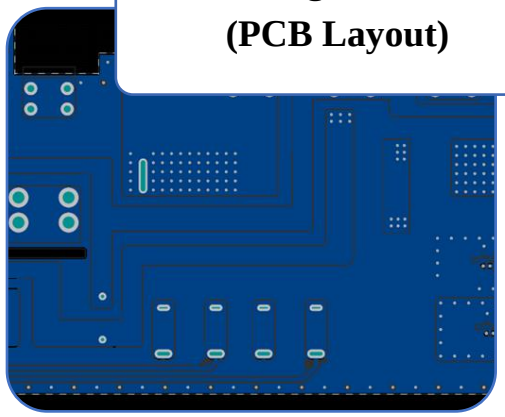
- The existing design displays unexpected peaks and drops in the output.
- The output fails to maintain a consistent 10V as intended.

How we executed?

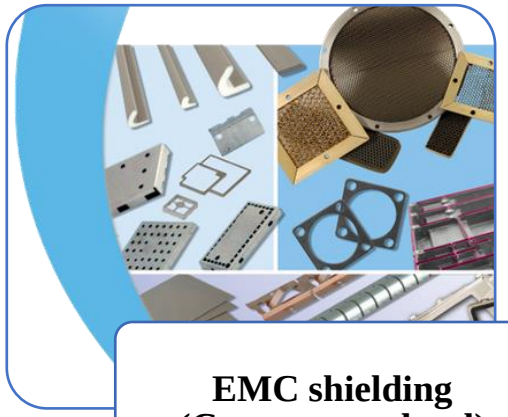
To reduce unwanted noise in monitoring points at the Outputs of Driver IC's U1 and U2, following are the design aspects at the different levels of design after observing the schematics and PCB of the existing project.



Design level (Schematics)



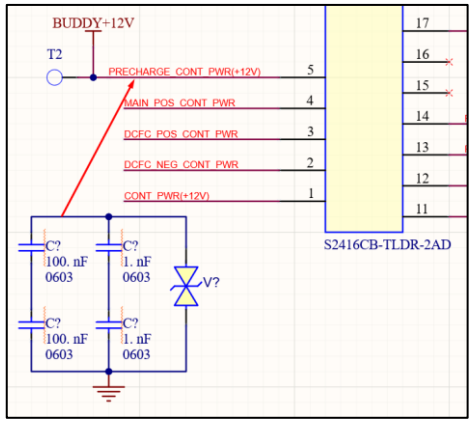
Design level (PCB Layout)



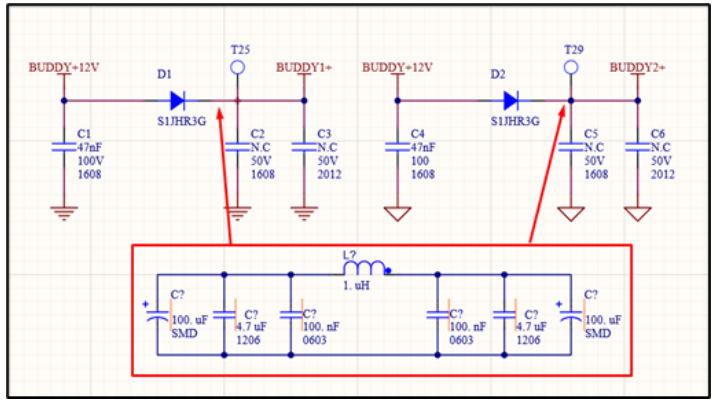
EMC shielding (Components level)

Design level (Schematics)

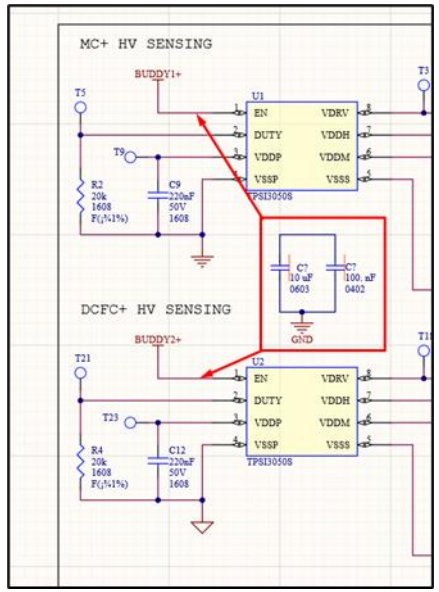
1. Adding the **TVS diode and capacitor filter section** near the Pin 5 of CON J1 will reduce the noise in entry level



2. Integrating the **PI filter sections** after the diodes (D1, D2) will reduce the Noise in Buddy signals

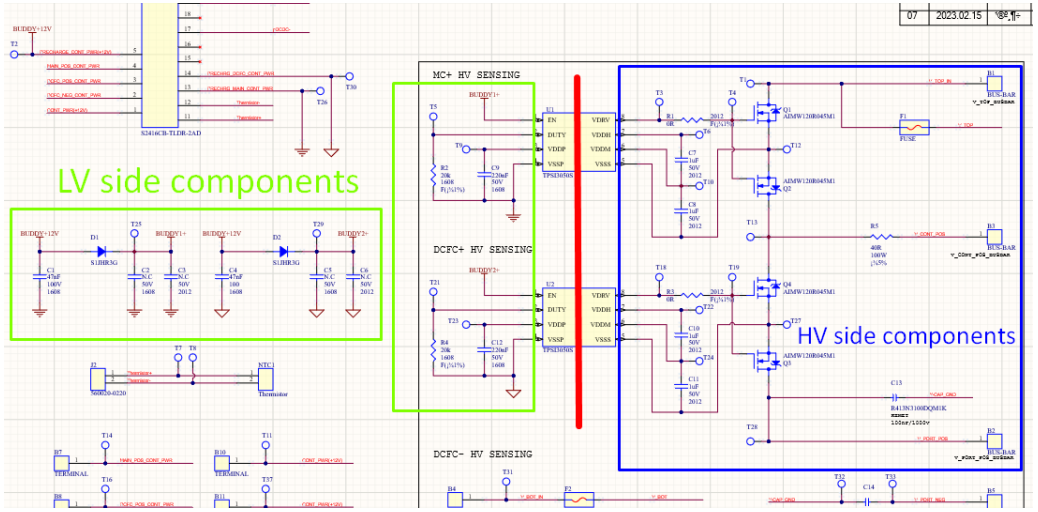


3. Placing the **Filter capacitors** near the EN pins of IC's (U1,U2) will filter the noise

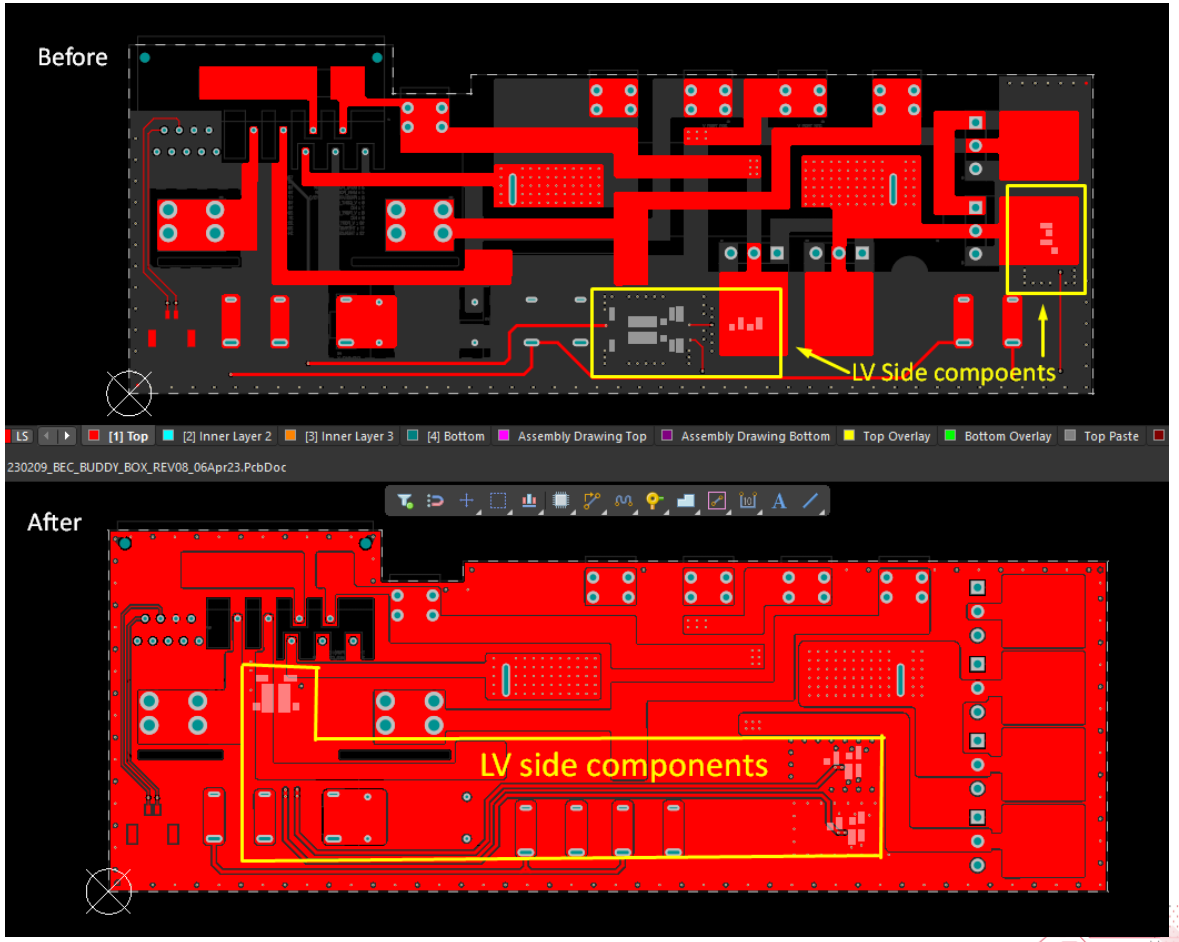


Design level (PCB Layout) (Cont.)

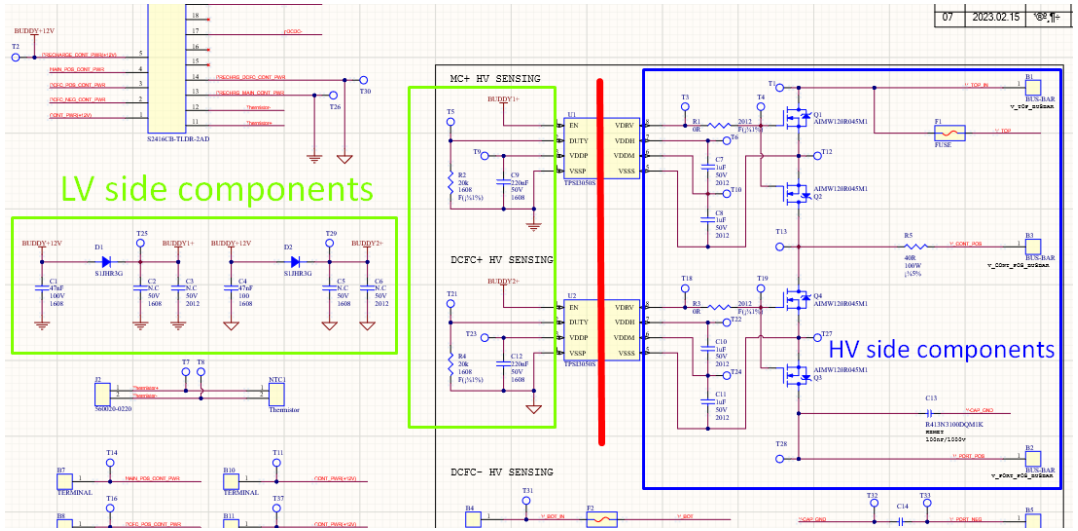
1. Placement of components based on HV Side and LV side.



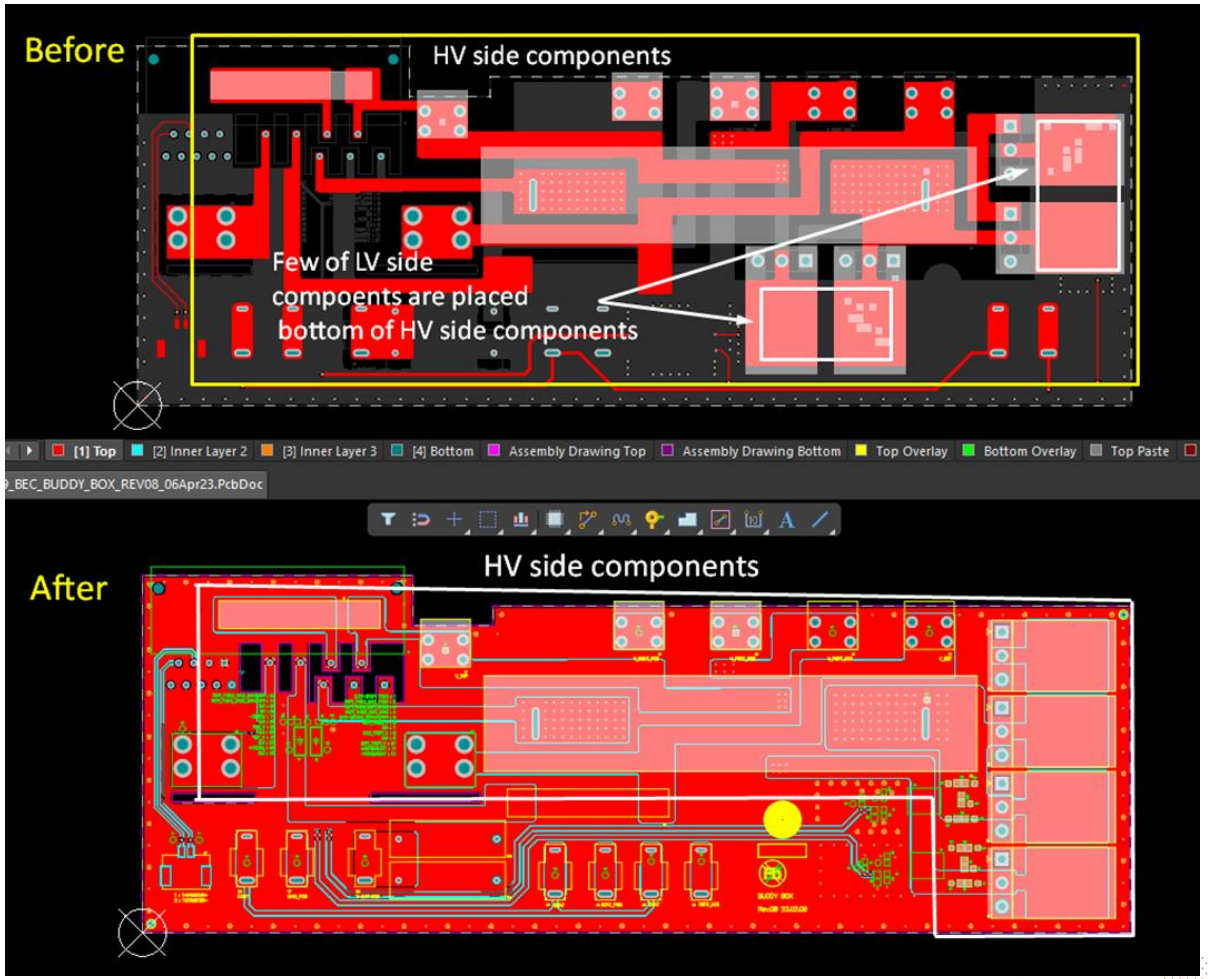
LV side components



Design level (PCB Layout)

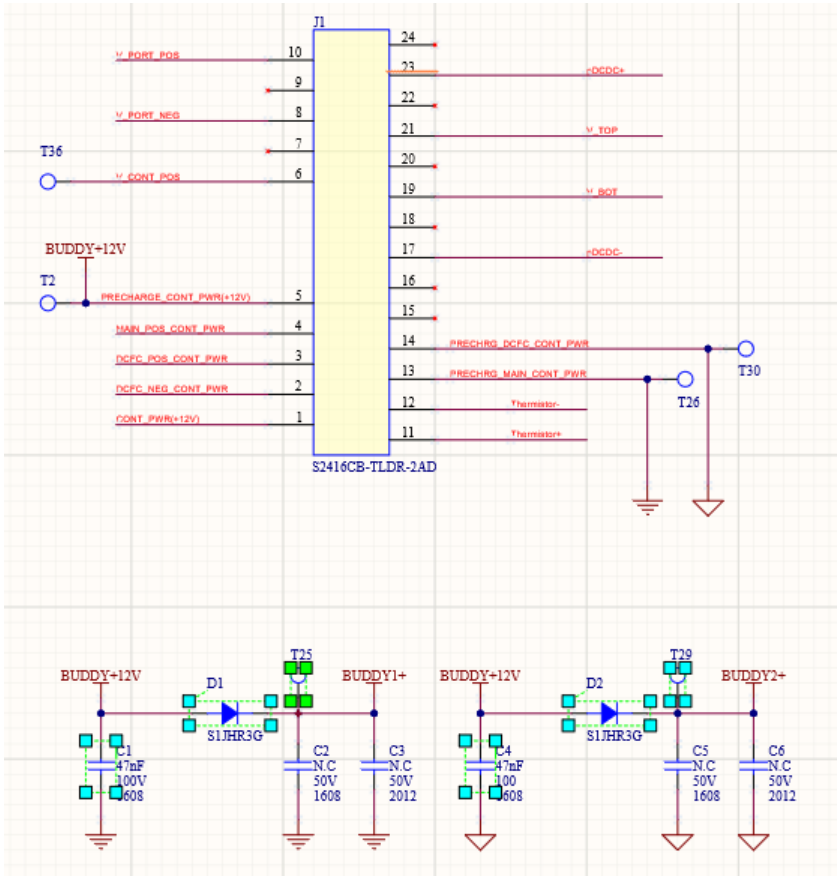


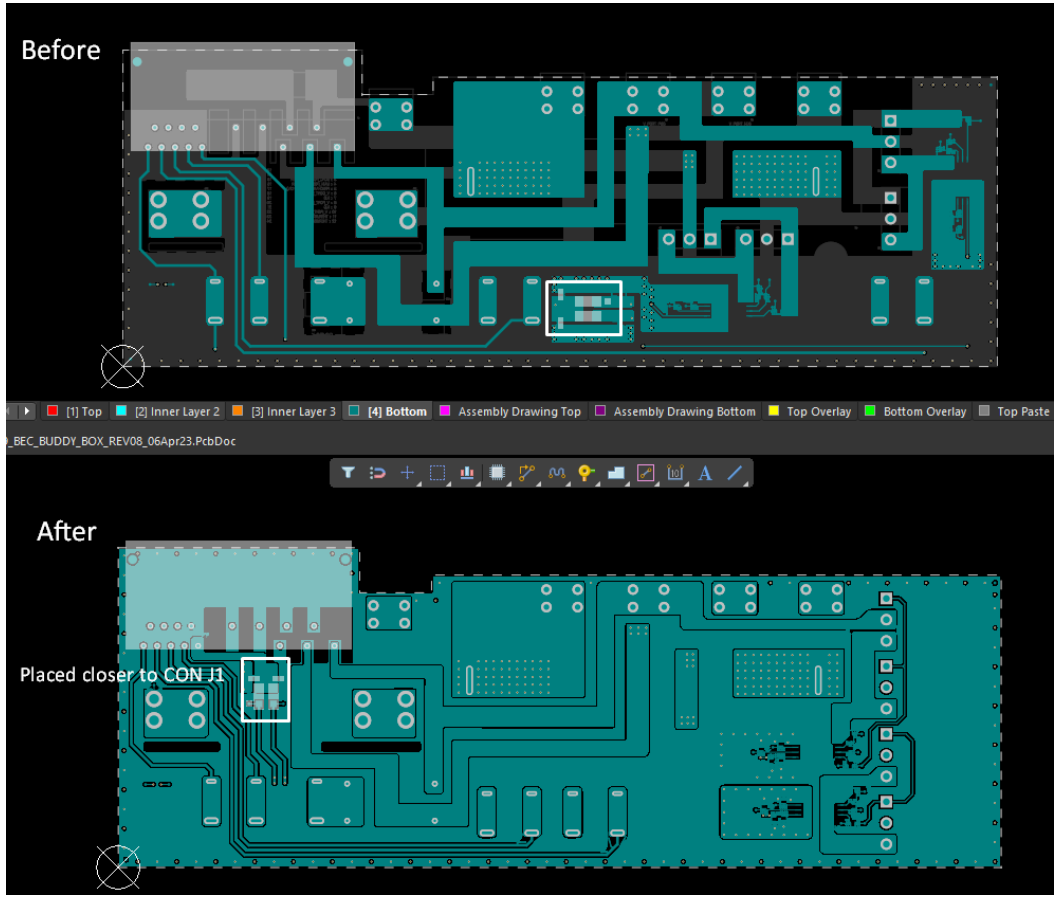
HV side components



Design level (PCB Layout)

2. **Power net (+12V) components** placed closer to CON J1





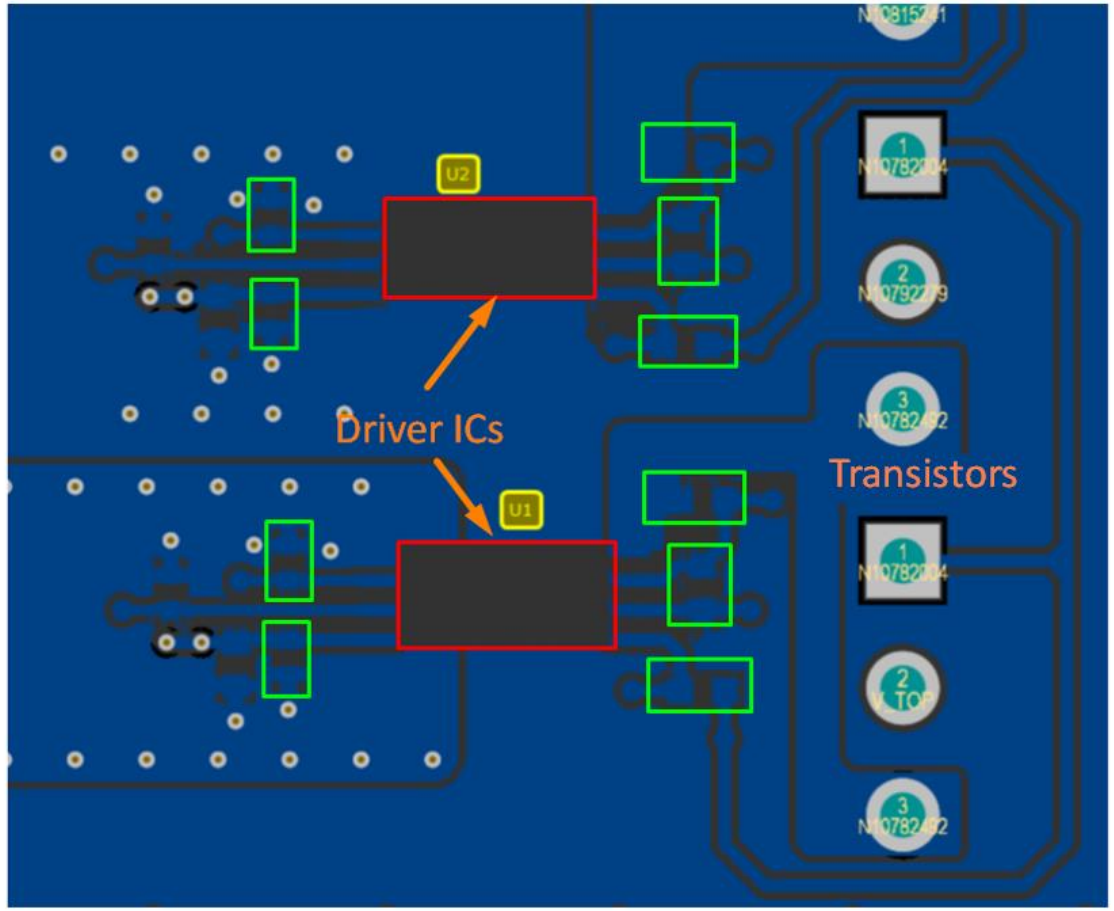
Design level (PCB Layout)

3. In Layout, placement and cu pour are implemented for Switch driver IC's(U1,U2) as per their **Layout recommendations.**

9.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI3050. Some key guidelines are:

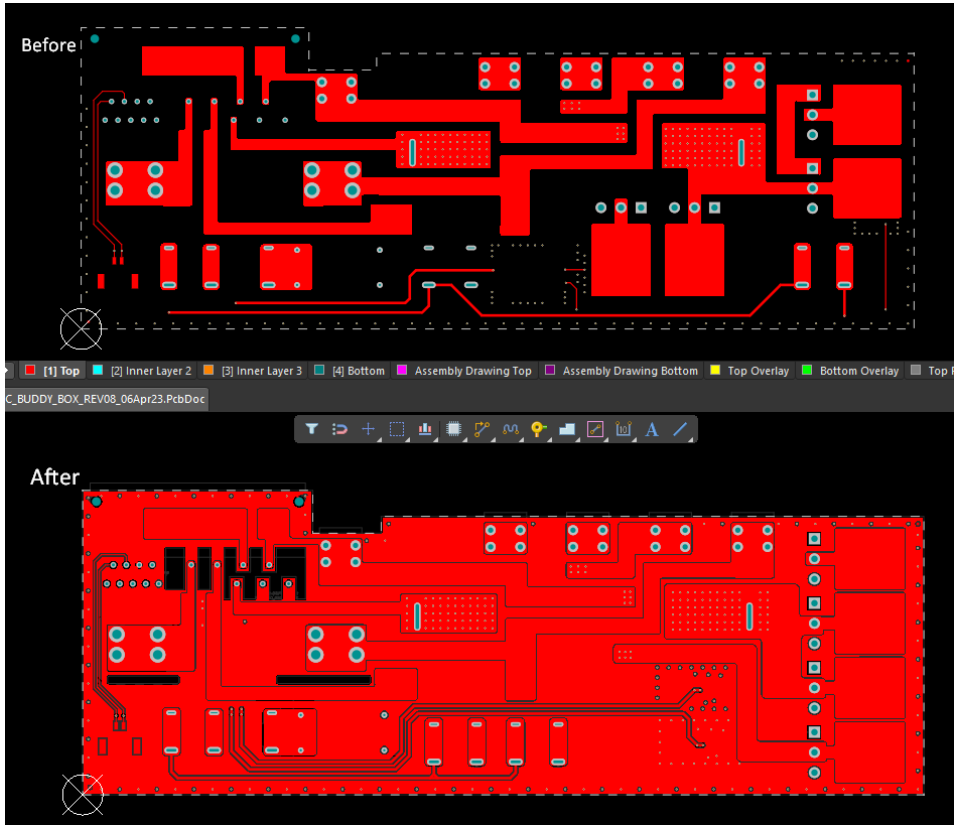
- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitances on the R_{PXFR} pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.



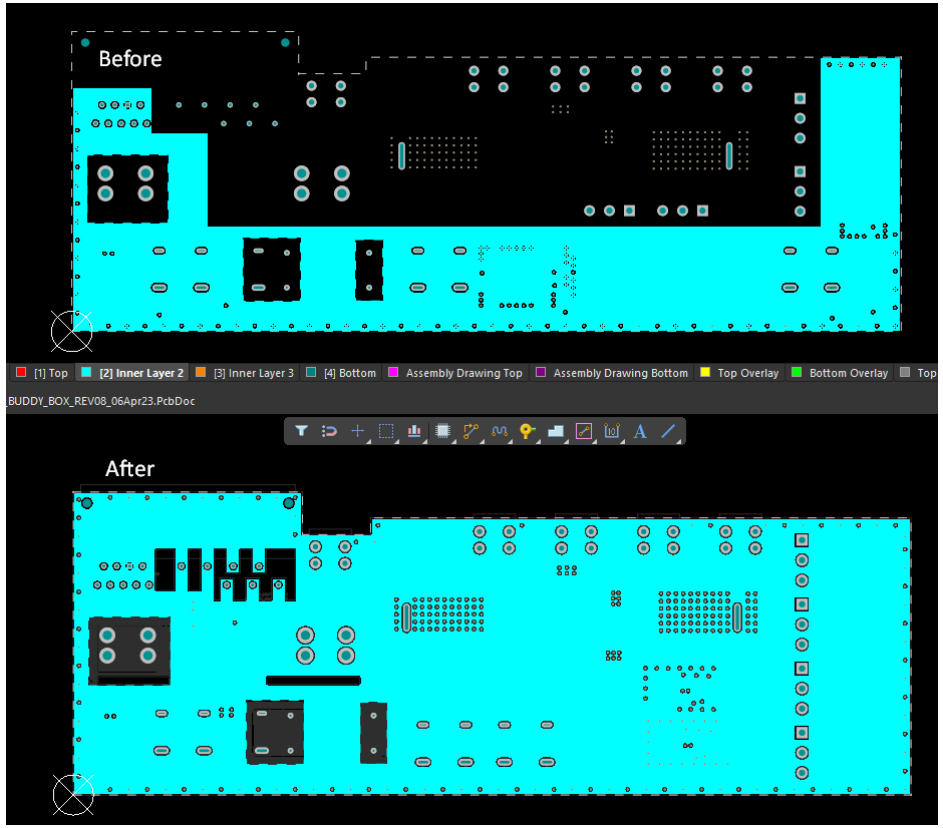
Design level (PCB Layout) (Cont.)

4. **GND** Cu poured on all layers for entire board

Layer 1



Layer 2



Design level (PCB Layout)

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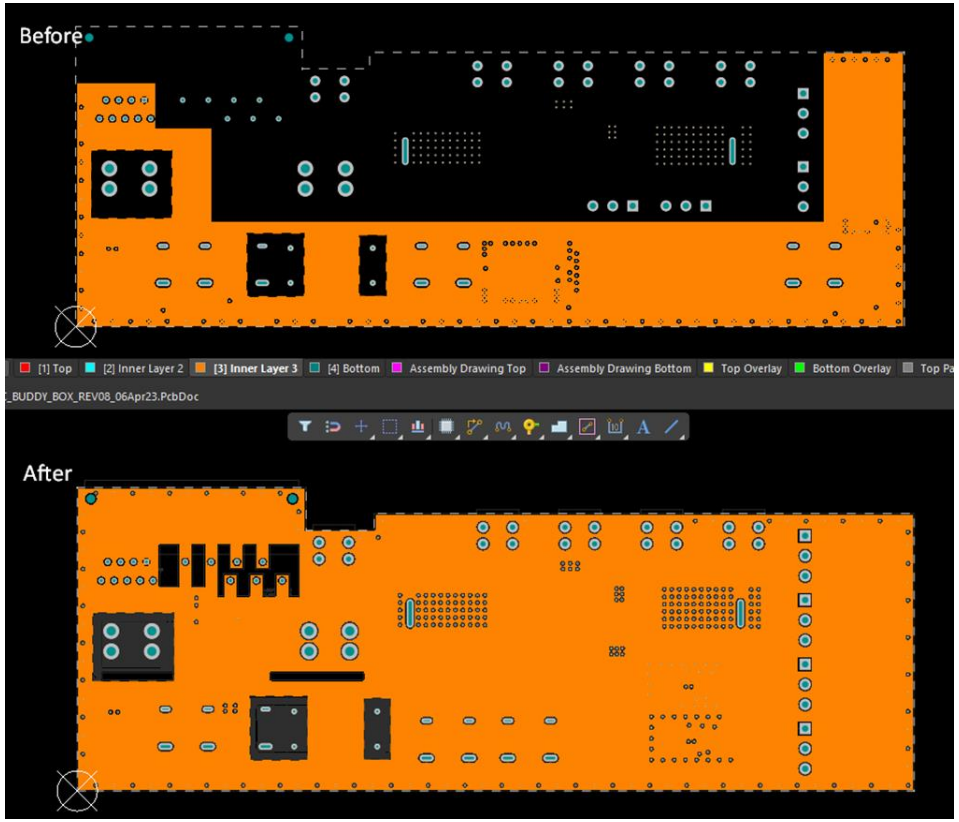
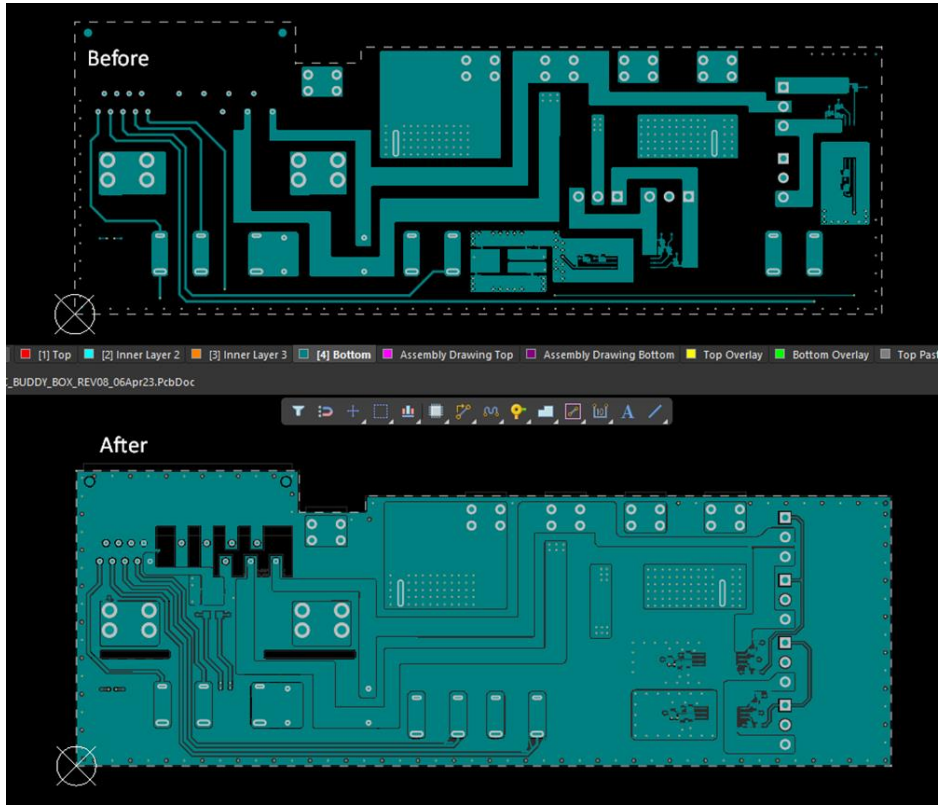
Layer 3

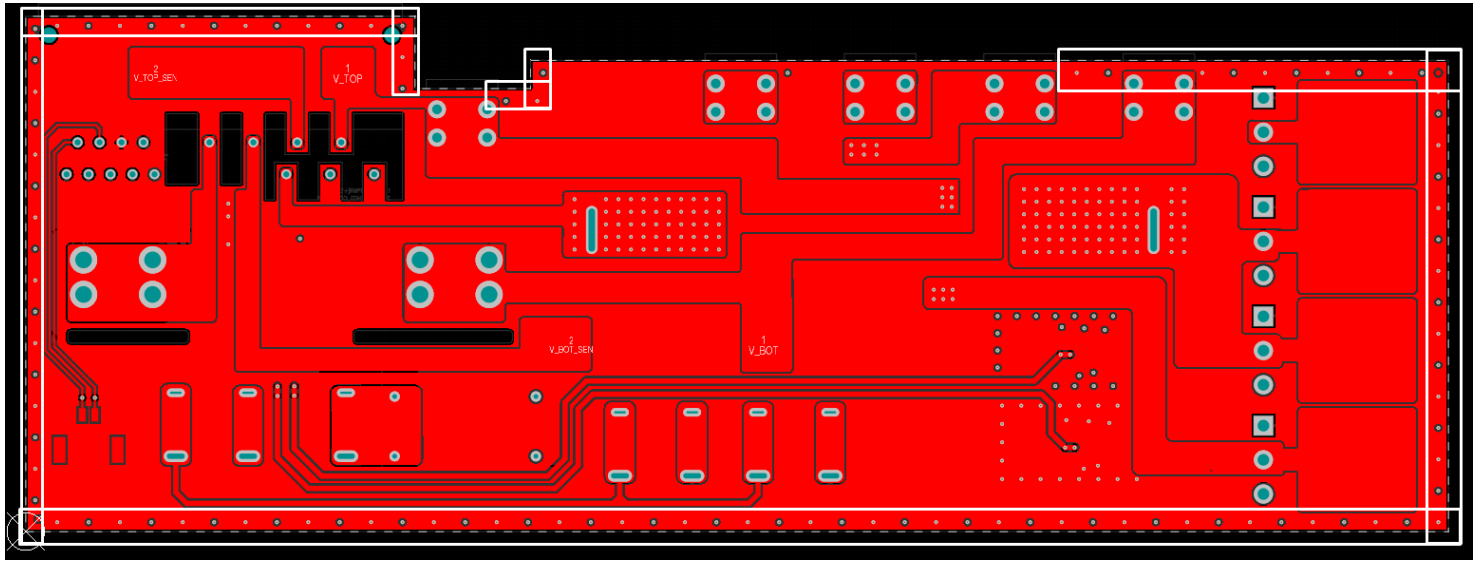


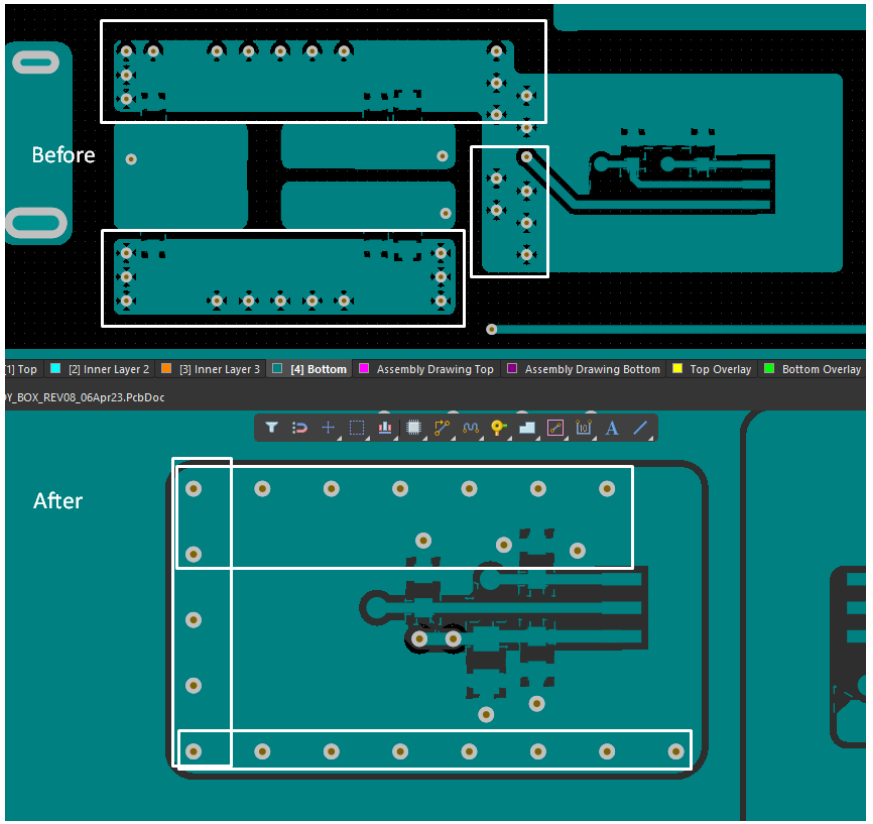
Layer 4



Design level (PCB Layout)

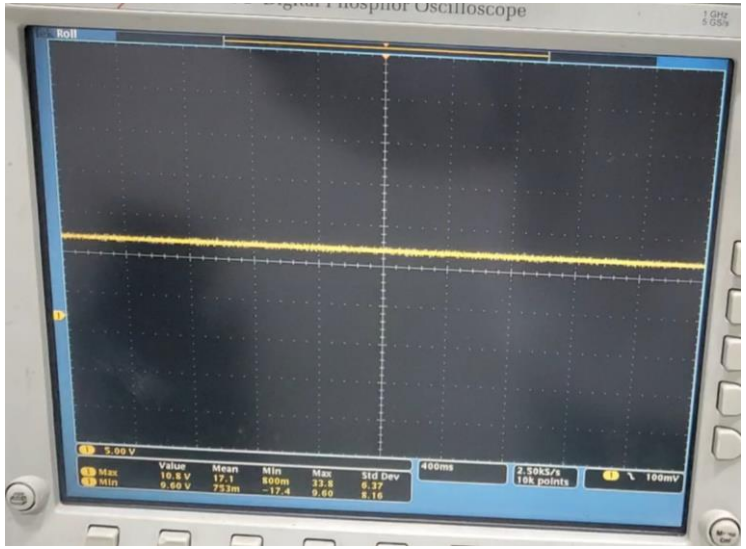
5. Connection between **Cu and Via are changed to Direct connect**. Also, **Vias are stitched** throughout PCB perimeter

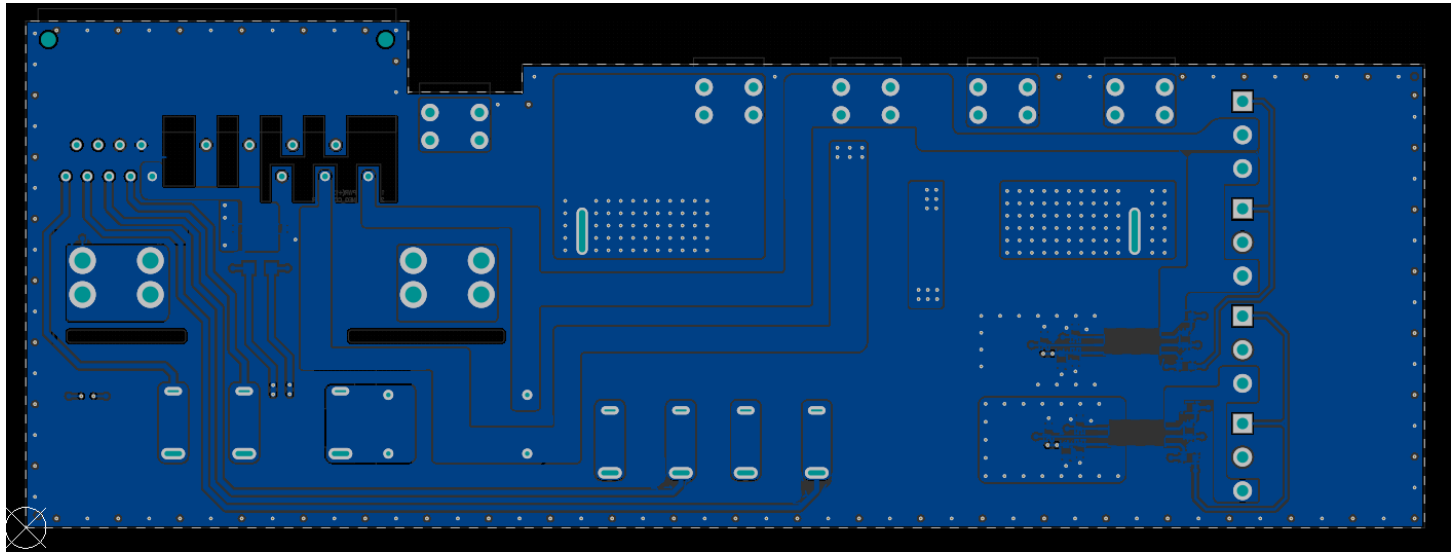




Proposed Design Analysis & results

Proposed Design Analysis output





- The proposed design displays expected output range from (9.6 to 10.8V) without peaks and drops in the output.
- The output pass to maintain a consistent 10V as intended.

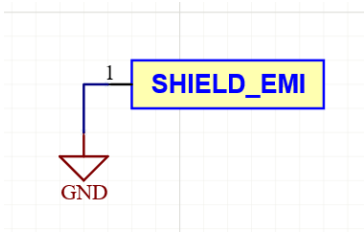
Value add

This particular outcome not only meets their specifications but also exceeds the Existing design, thereby contributing significant value to the overall pre-charging circuit in the Battery Management System (BMS).

EMC shielding (Components level)

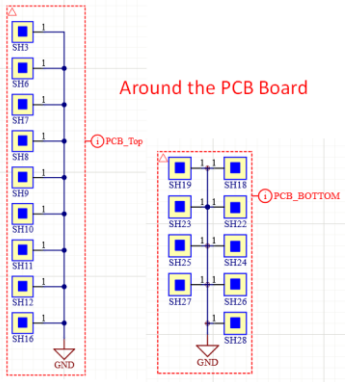
Suggestion:

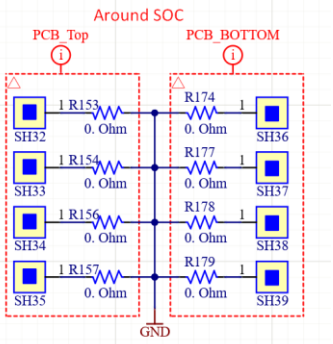
- Implementing(EMI/EMC shields or gaskets around EMC-sensitive components, as illustrated in the provided images

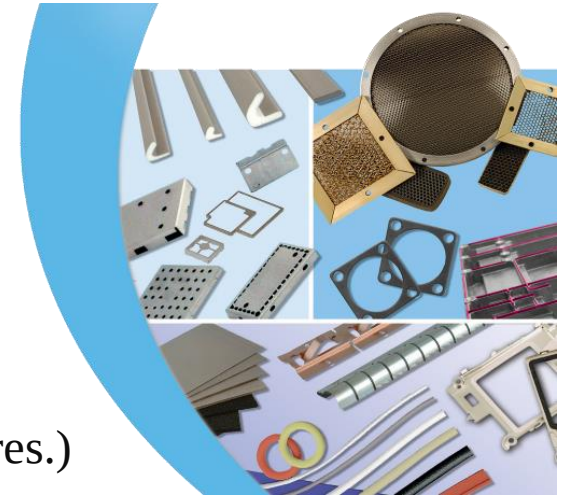


- Consider placing **spring clips or fingers** around both the top and bottom layers of the PCB board.

Spring clips







(If design level methods prove ineffective, consider integrating the mentioned features.)
Consider using upcoming power boards while also incorporating the mentioned features.

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Client Testimonial

Presented here is a testimonial from a satisfied client, serving as strong evidence of the successful resolution of EMI/EMC issues.

"We express our utmost satisfaction with the outstanding performance of this exceptional team. Faced with numerous challenges, they skillfully crafted our circuit design, effectively mitigating EMI/EMC issues. Their design reflects a seamless integration of creativity and engineering expertise in their services. What sets them apart is their unwavering commitment to delivering a cost-efficient design without compromising quality. Within a surprisingly short timeframe, they not only met but exceeded our expectations, reaching a significant milestone in our project. This team has proven to be the preferred choice for those seeking a winning combination of timeliness, affordability, and excellence."

Conclusion

Our dedication to excellence and technical expertise was evident in the successful delivery of EMI/EMC handling tailored to meet the client's requirements.

Our partnership seamlessly combines expertise with personalized service, complemented by technical proficiency.

Our commitment is evident in delivering excellent EMI/EMC handling in PCB layouts, not just reducing costs but also showcasing our capability and dependability in consistently achieving outstanding results. Central to our approach is the emphasis on quality and strict adherence to timelines