

Signal Integrity Analysis

Scope : Enhance Signal Reliability and Optimize Performance

Application : Advanced Driver Assistance Systems

In automotive applications, signal integrity practices are essential for safety and driver-assistance systems. By integrating these practices into PCB layout, signal quality is preserved as it travels from driver components to receivers.

Signal integrity analysis is critical for ADAS application boards, ensuring reliable and accurate performance across various functions. It helps enhance signal quality, reduce distortions, and address challenges like crosstalk and timing issues. This analysis is particularly important for ADAS applications, where precise signal transmission is vital for optimal functionality and safety.



Signal Integrity Analysis - Challenges

The client has asked for a signal integrity analysis of the layout to ensure top performance. Here, we outline the challenges involved in Signal Integrity Analysis.

Challenges

- ◆ Cross Talk
- ◆ Ground Bounce
- ◆ Reflections and Impedance Mismatch
- ◆ Skew and Timing
- ◆ Signal Termination
- ◆ High-Frequency Effects
- ◆ Via Impacts
- ◆ Power Distribution
- ◆ Noise & EMI effects
- ◆ Continuous reference planes



Signal Integrity Analysis - SoW



01

Analyzing High-Speed Signal Groups
Listing Impedance and Requirements



03

Performance Analysis
Plot and Outcome Review



05

Implementations
Layout Design Modifications



02

Analysis -Hyper Lynx
Essential Parameters Identification



04

Recommendations
To enhance Performance



Study of High Speed Signals / Groups

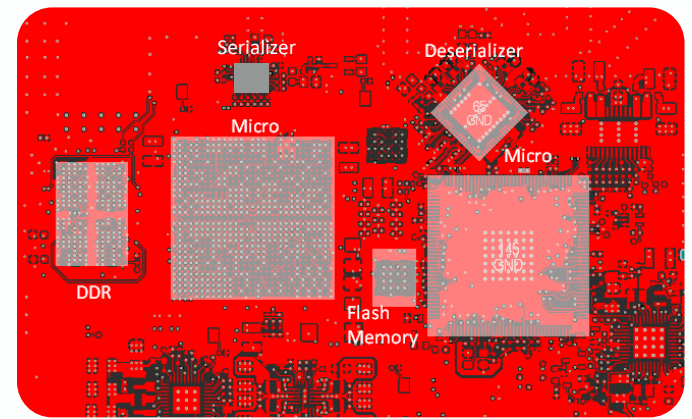
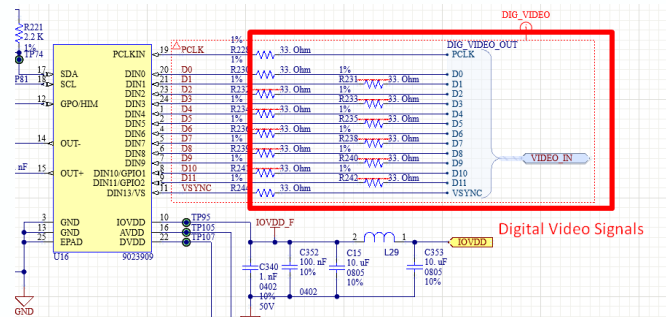
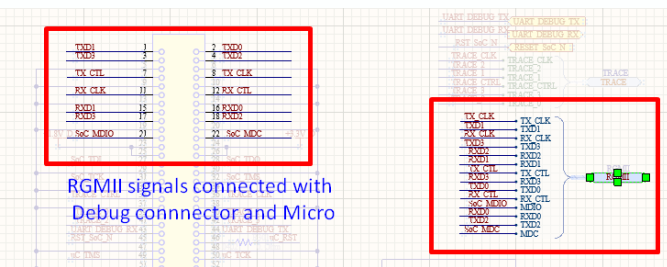
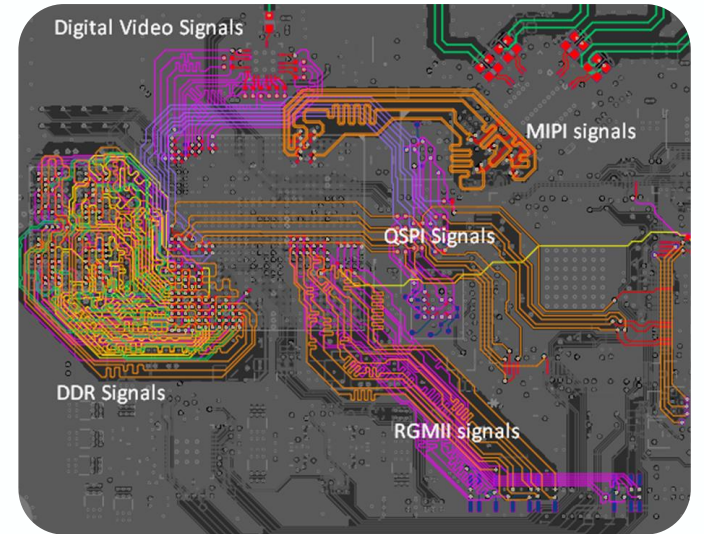
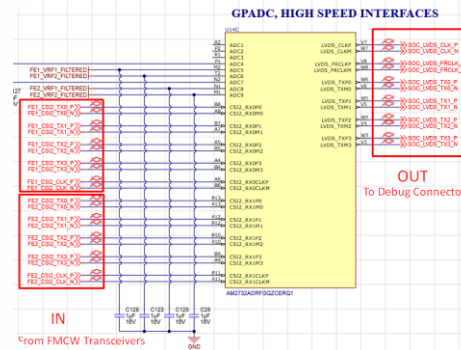
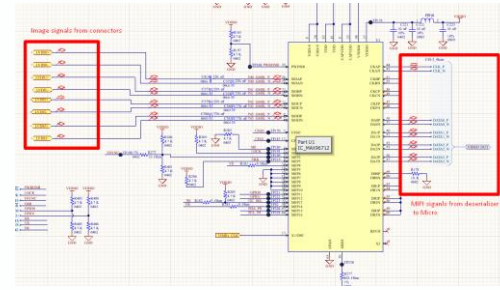
The High Speed Signal circuits in the project are studied thoroughly to evaluate the performance.

High Speed Signals

- MIPI - DeSerializer to SoC
- DDR - DDR to SoC
- RGMII - SoC to Debug connector
- DIG_VIDEO – SoC to Serializer
- QSPI – SoC to Flash memory

High Speed Signal Circuits

- SoC & DDR.
- Serializer & DeSerializer
- Debug Connector
- Flash memory



Analysis Execution

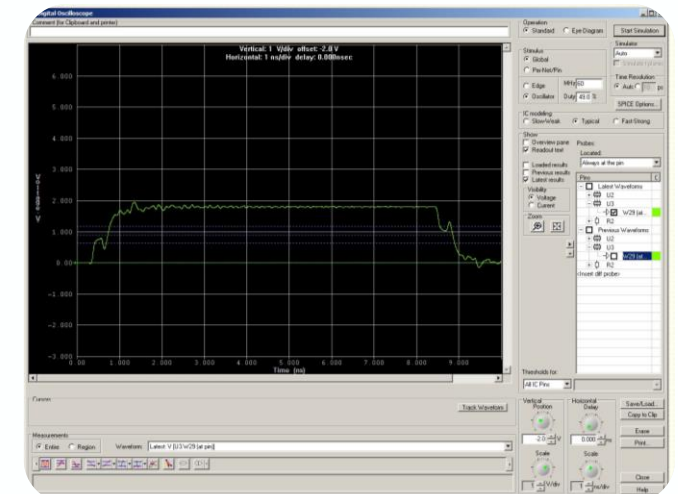
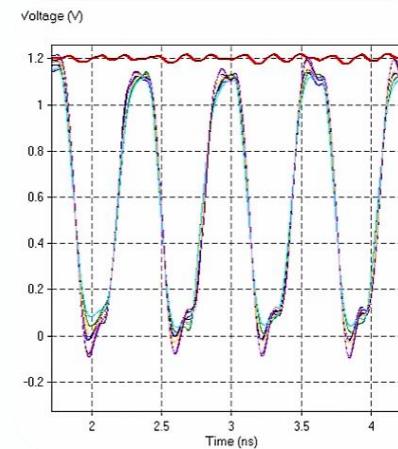
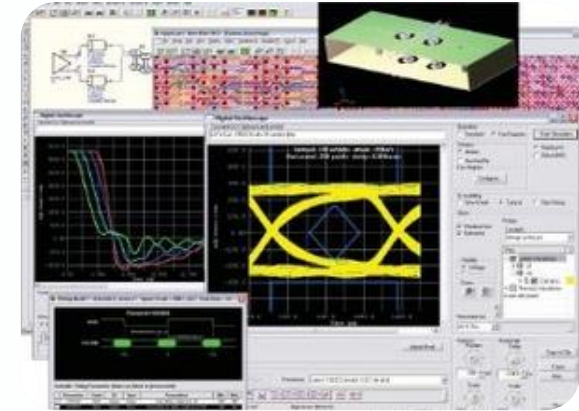
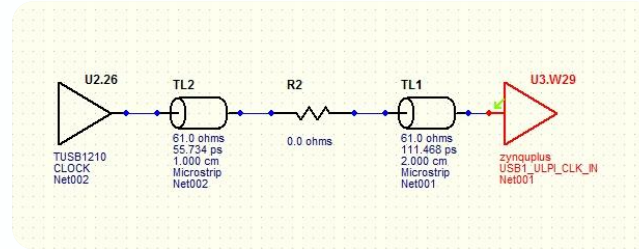
We conducted a signal integrity analysis using the **HyperLynx** tool to assess the performance of the layout.

Signal Integrity issues were detected at two levels:

- Interconnect level and
- Systems-level

Quantities to calculate include:

- ✓ Impedance Matching.
- ✓ Interactions between the PDN and high-speed signals.
- ✓ Jitter Analysis.
- ✓ Return path discontinuities.
- ✓ Result of Simultaneous Switching Noise (SSN).

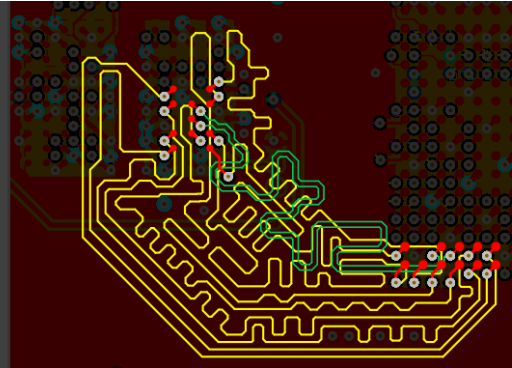


Analysis Execution (Cont.)

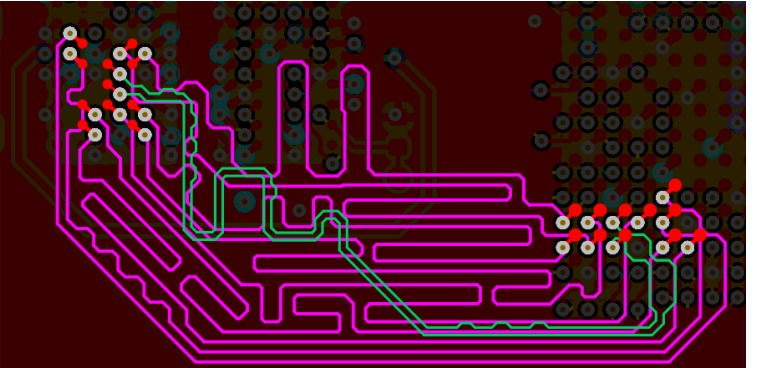
DDR signals – DDR to SoC

Layout - Routing

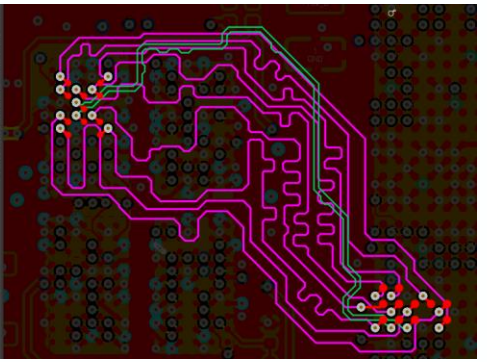
Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...
B_1_DQ0	2	2072.114	727.016	Net is Hii	134
B_1_DQ1	2	2068.1	731.539	Net is Hii	133
B_1_DQ2	2	2082.2	714.759	Net is Hii	133
B_1_DQ3	2	2069.731	721.337	Net is Hii	134
B_1_DQ4	2	2093.962	565.231	Net is Hii	152
B_1_DQ5	2	2078.781	581.661	Net is Hii	145
B_1_DQ6	2	2073.539	603.905	Net is Hii	144
B_1_DQ7	2	2071.721	564.77	Net is Hii	152
B_DM1	2	2072.639	619.486	Net is Hii	145
B_DM1	2	2072.639	619.486	Net is Hii	145
B_DQS1_N	2	2066.479	643.019	Net is Hii	144
B_DQS1_N	2	2066.479	643.019	Net is Hii	144
B_DQS1_P	2	2073.361	640.885	Net is Hii	144
B_DQS1_P	2	2073.361	640.885	Net is Hii	144



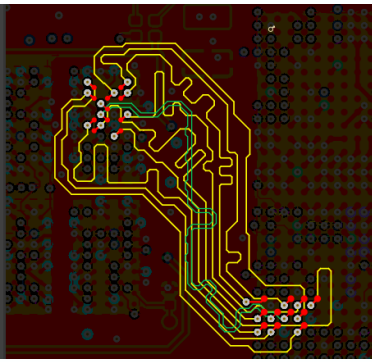
Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...
B_0_DQ0	2	2076.044	572.759	Net is Hii	150
B_0_DQ1	2	2072.193	569.88	Net is Hii	150
B_0_DQ2	2	2065.845	576.307	Net is Hii	148
B_0_DQ3	2	2091.018	561.72	Net is Hii	152
B_0_DQ4	2	2074.09	688.004	Net is Hii	127
B_0_DQ5	2	2099.207	683.8	Net is Hii	138
B_0_DQ6	2	2078.071	686.155	Net is Hii	139
B_0_DQ7	2	2074.936	667.592	Net is Hii	140
B_DM0	2	2077.2	622.98	Net is Hii	145
B_DM0	2	2077.2	622.98	Net is Hii	145
B_DQS0_N	2	2069.616	697.853	Net is Hii	137
B_DQS0_N	2	2069.616	697.853	Net is Hii	137
B_DQS0_P	2	2076.796	700.011	Net is Hii	141
B_DQS0_P	2	2076.796	700.011	Net is Hii	141



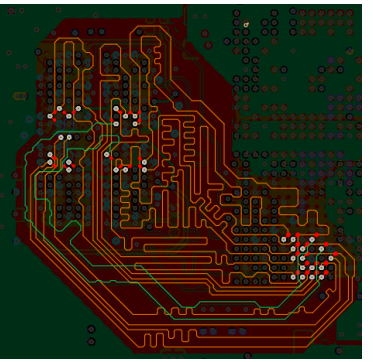
Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...
A_0_DQ0	2	1882.825	814.072	Net is Hii	134
A_0_DQ1	2	1879.168	494.063	Net is Hii	138
A_0_DQ2	2	1875.768	491.932	Net is Hii	138
A_0_DQ3	2	1878.419	473.368	Net is Hii	146
A_0_DQ4	2	1879.566	562.055	Net is Hii	131
A_0_DQ5	2	1871.778	532.021	Net is Hii	133
A_0_DQ6	2	1872.337	527.793	Net is Hii	135
A_0_DQ7	2	1877.643	571.418	Net is Hii	136
A_DM0	2	1878.983	533.285	Net is Hii	132
A_DM0	2	1878.983	533.285	Net is Hii	132
A_DQS0_N	2	1874.469	536.752	Net is Hii	133
A_DQS0_N	2	1874.469	536.752	Net is Hii	133
A_DQS0_P	2	1883.006	541.406	Net is Hii	134
A_DQS0_P	2	1883.006	541.406	Net is Hii	134



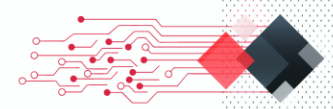
Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...
A_1_DQ0	2	1760.751	532.092	Net is Hii	122
A_1_DQ1	2	1760.279	553.048	Net is Hii	120
A_1_DQ2	2	1760.656	540.705	Net is Hii	121
A_1_DQ3	2	1757.995	541.861	Net is Hii	123
A_1_DQ4	2	1760.029	571.95	Net is Hii	118
A_1_DQ5	2	1759.237	581.578	Net is Hii	117
A_1_DQ6	2	1766.041	532.781	Net is Hii	123
A_1_DQ7	2	1755.329	595.345	Net is Hii	115
A_DM1	2	1764.321	491.022	Net is Hii	127
A_DM1	2	1764.321	491.022	Net is Hii	127
A_DQS1_N	2	1752.272	560.919	Net is Hii	119
A_DQS1_N	2	1752.272	560.919	Net is Hii	119
A_DQS1_P	2	1760.901	554.871	Net is Hii	120
A_DQS1_P	2	1760.901	554.871	Net is Hii	120



Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...
A_Adr0	2	2422.993	449.746	Net is Hii	191
A_Adr1	2	2431.824	436.918	Net is Hii	195
A_Adr2	2	2429.646	470.33	Net is Hii	191
A_Adr3	2	2433.744	458.932	Net is Hii	191
A_Adr4	2	2401.93	419.861	Net is Hii	194
A_Adr5	2	2437.968	440.371	Net is Hii	195
A_CLK_P	2	2419.734	453.284	Net is Hii	194
B_Adr0	2	2528.422	394.015	Net is Hii	211
B_Adr1	2	2531.03	492.673	Net is Hii	202
B_Adr2	2	2508.91	549.604	Net is Hii	191
B_Adr3	2	2499.536	506.136	Net is Hii	191
B_Adr4	2	2526.883	514.447	Net is Hii	201
B_Adr5	2	2538.219	538.722	Net is Hii	195
B_CLK_P	2	2593.284	449.894	Net is Hii	209
LPDDR4_CS0	3	n/a	408.237	Net is Hii	224
LPDDR4_CS1	3	n/a	529.352	Net is Hii	211



CLK and Data's are routed with same trace length(closely)



Analysis Execution (Cont.)

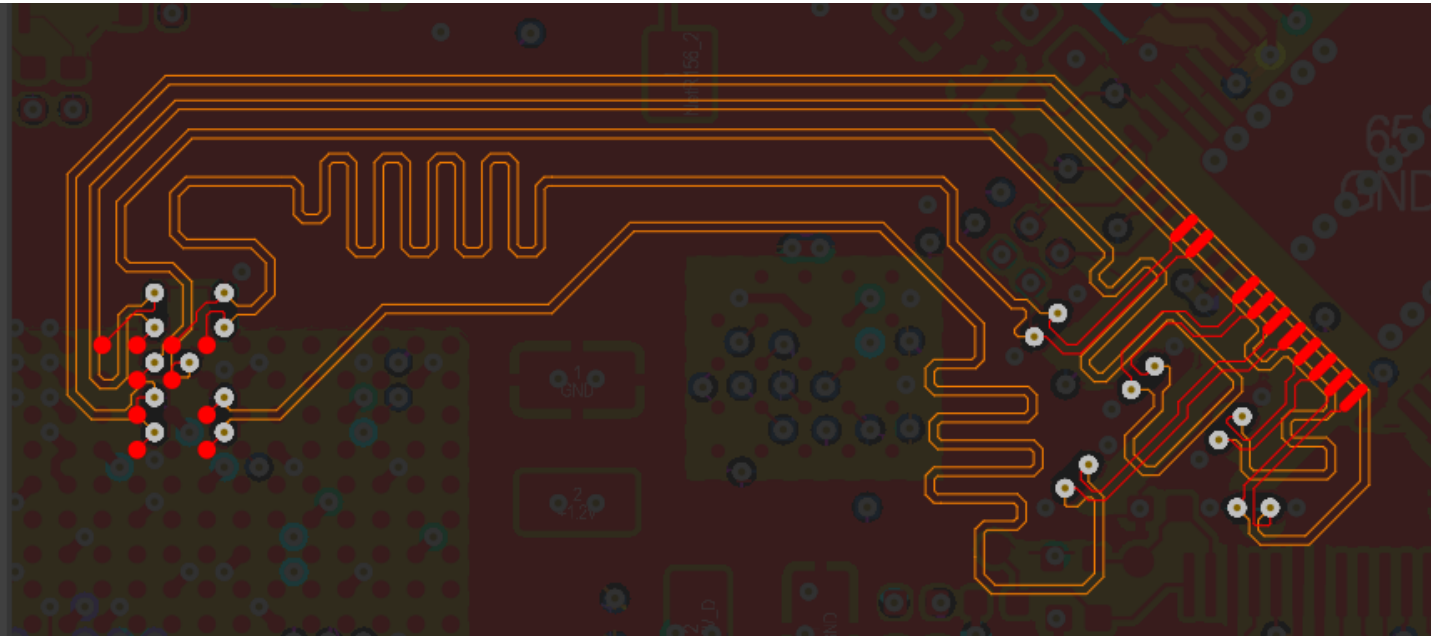
MIPI signals – DeSerializer to SoC

Layout - Routing

Trace Lengths

Layer 3

10 Nets (0 Highlighted)						
* Name	Nod...	Signal Leng...	Total Pin...	Unrou...	R...	
<input type="checkbox"/> CAM_MIPI_CLK_N	2	2060	0	Net is Hi	206	
<input type="checkbox"/> CAM_MIPI_CLK_P	2	2059.475	0	Net is Hi	205	
<input type="checkbox"/> CAM_MIPI_D0_N	2	2060	0	Net is Hi	206	
<input type="checkbox"/> CAM_MIPI_D0_P	2	2059.286	0	Net is Hi	205	
<input type="checkbox"/> CAM_MIPI_D1_N	2	2060	0	Net is Hi	206	
<input type="checkbox"/> CAM_MIPI_D1_P	2	2059.02	0	Net is Hi	205	
<input type="checkbox"/> CAM_MIPI_D2_N	2	2060	0	Net is Hi	206	
<input type="checkbox"/> CAM_MIPI_D2_P	2	2059.215	0	Net is Hi	205	
<input type="checkbox"/> CAM_MIPI_D3_N	2	2059.078	0	Net is Hi	205	
<input type="checkbox"/> CAM_MIPI_D3_P	2	2058.006	0	Net is Hi	205	



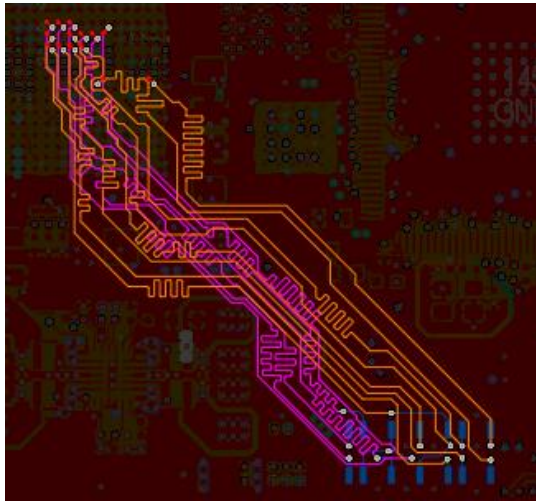
CLK and Data's are routed with same trace length (closely)



Analysis Execution (Cont.)

Layout - Routing

RGMIi signals – DeSerializer to SoC

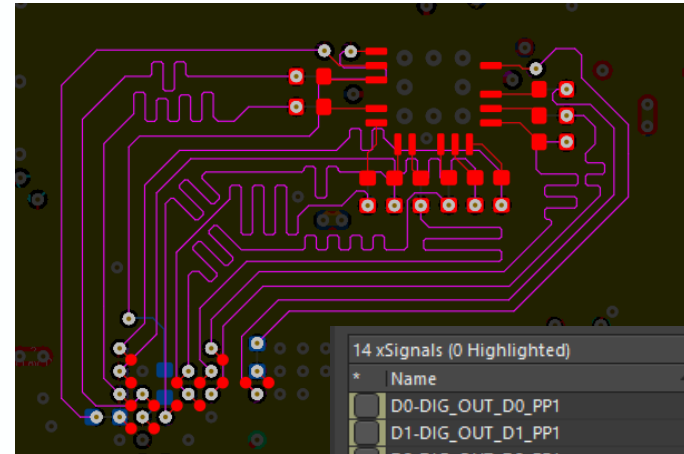


Trace Lengths

14 Nets (0 Highlighted)						
* Name	Nod...	Signal Len...	Total Pl...	Unrou...	R...	
RGMIi.MDC	2	2249.999	0	Net is Hi...	224	
RGMIi.MDIO	2	2249.999	0	Net is Hi...	224	
RGMIi.RXD0	2	2250.001	0	Net is Hi...	225	
RGMIi.RXD1	2	2250	0	Net is Hi...	224	
RGMIi.RXD2	2	2249.999	0	Net is Hi...	224	
RGMIi.RXD3	2	2250	0	Net is Hi...	224	
RGMIi.RX_CLK	2	2249.999	0	Net is Hi...	224	
RGMIi.RX_CTL	2	2249.999	0	Net is Hi...	225	
RGMIi.TXD0	2	2249.999	0	Net is Hi...	225	
RGMIi.TXD1	2	2251.025	0	Net is Hi...	225	
RGMIi.TXD2	2	2250.001	0	Net is Hi...	224	
RGMIi.TXD3	2	2250.001	0	Net is Hi...	224	
RGMIi.TX_CLK	2	2249.999	0	Net is Hi...	225	
RGMIi.TX_CTL	2	2250	0	Net is Hi...	224	

CLK and Data's are routed with same trace length (closely)

DIG_VIDEO signals – SoC to Serializer



Trace Lengths

14 xSignals (0 Highlighted)						
* Name	Node ...	Signal Length (...)	T...	R...	U...	
D0-DIG_OUT_D0_PP1	4	1099.692	0	109	0	
D1-DIG_OUT_D1_PP1	4	1100.001	0	110	0	
D2-DIG_OUT_D2_PP1	4	1102.539	0	110	0	
D3-DIG_OUT_D3_PP1	4	1100.305	0	110	0	
D4-DIG_OUT_D4_PP1	4	1100.001	0	110	0	
D5-DIG_OUT_D5_PP1	4	1100.036	0	110	0	
D6-DIG_OUT_D6_PP1	4	1100.145	0	110	0	
D7-DIG_OUT_D7_PP1	4	1100.267	0	110	0	
D8-DIG_OUT_D8_PP1	4	1100	0	110	0	
D9-DIG_OUT_D9_PP1	4	1100.145	0	110	0	
D10-DIG_OUT_D10_PP1	4	1100.001	0	110	0	
D11-DIG_OUT_D11_PP1	4	1100.107	0	110	0	
PCLK-DIG_OUT_PCLK_PP1	4	1101.372	0	110	0	
VSYNC-DIG_OUT_VSYNC_PP1	4	1100.153	0	110	0	



Analysis - Plots and Results

Topology – MIPI-CLK



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

$$V_{inH} = 740mV$$

$$V_{inL} = 550mV$$

High Speed Mode:

$$V_{inH} = 460mV$$

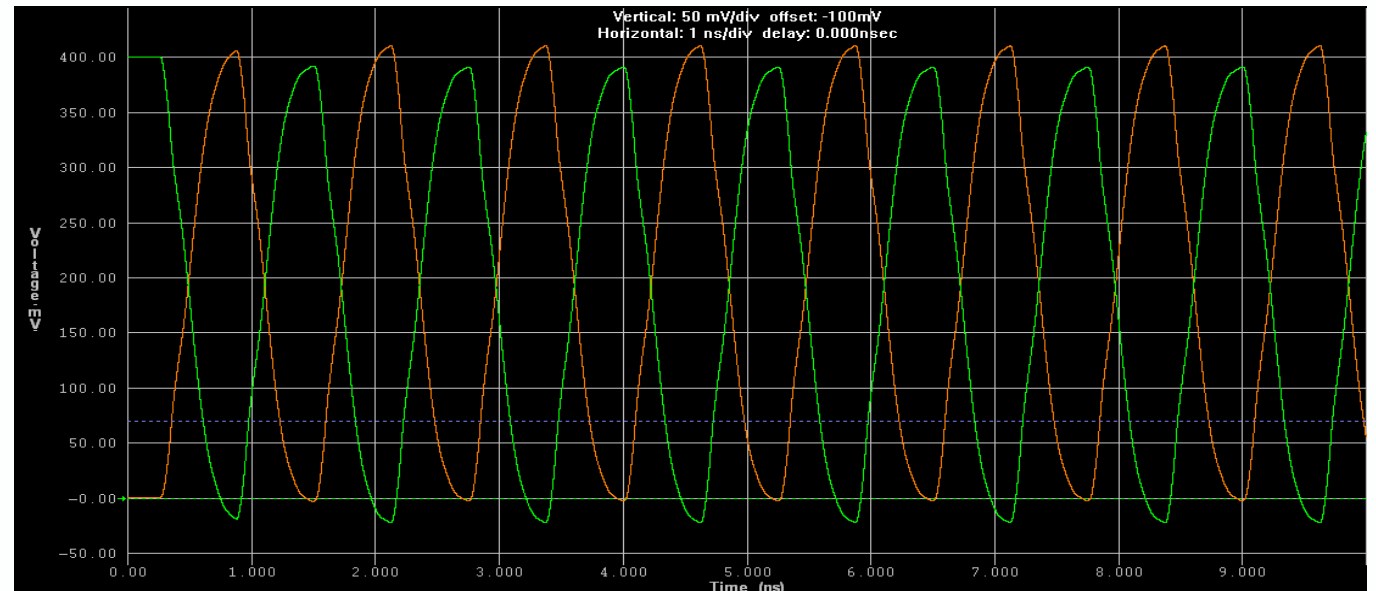
$$V_{inL} = 40mV$$

MIPI interface standard requirements

$$V_{inH} = 235mV$$

$$V_{inL} = 165mV$$

Analysis Result

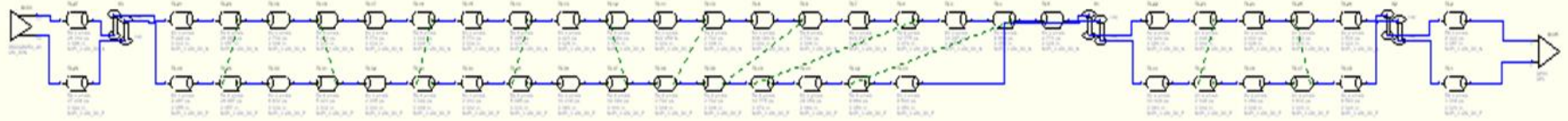


Both values meet the requirements, resulting in a **pass**.



Analysis - Plots and Results (Cont.)

Topology - MIPI - DATA



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

$$V_{inH} = 700mV$$

$$V_{inL} = 500mV$$

High Speed Mode:

$$V_{inH} = 300V$$

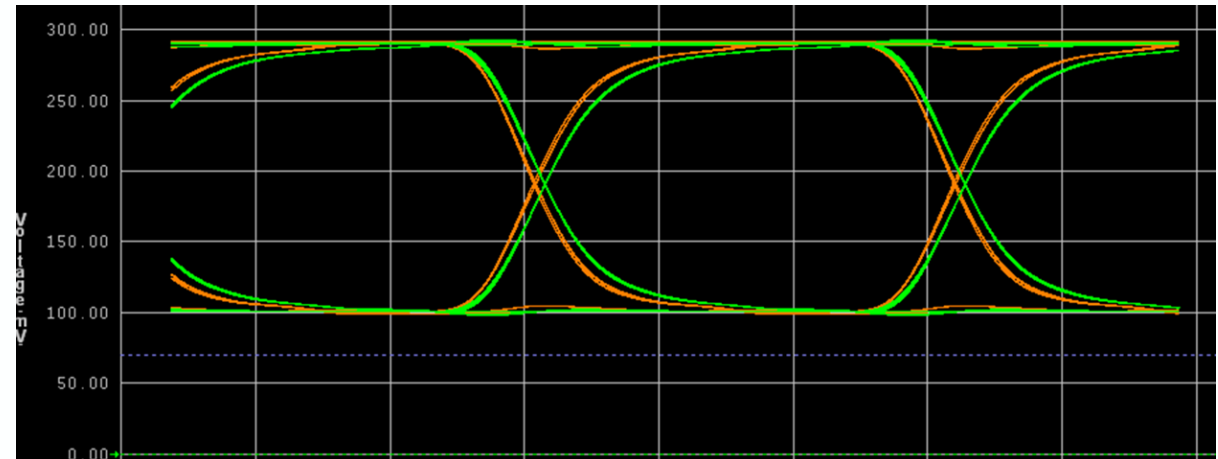
$$V_{inL} = 60mV$$

MIPI interface standard requirements

$$V_{inH} = 205mV$$

$$V_{inL} = 145mV$$

Analysis Result

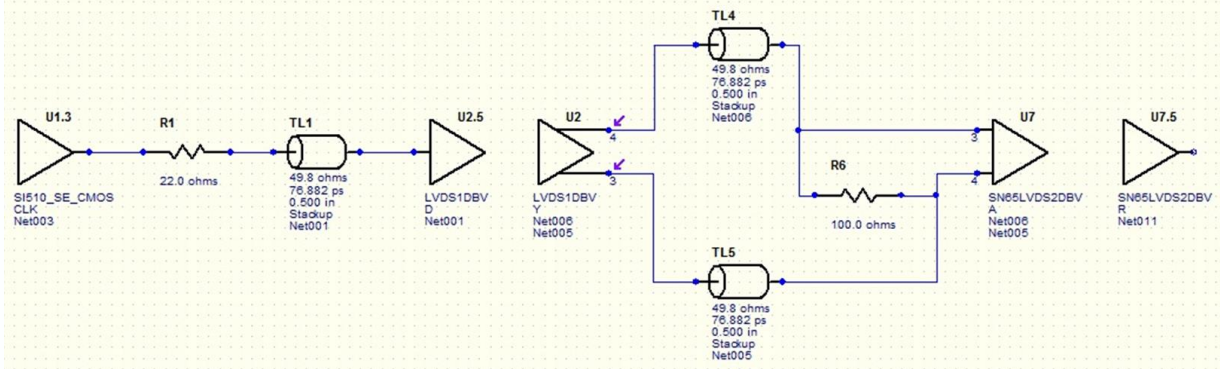


Both the values are meeting the requirement and the results are **pass**.

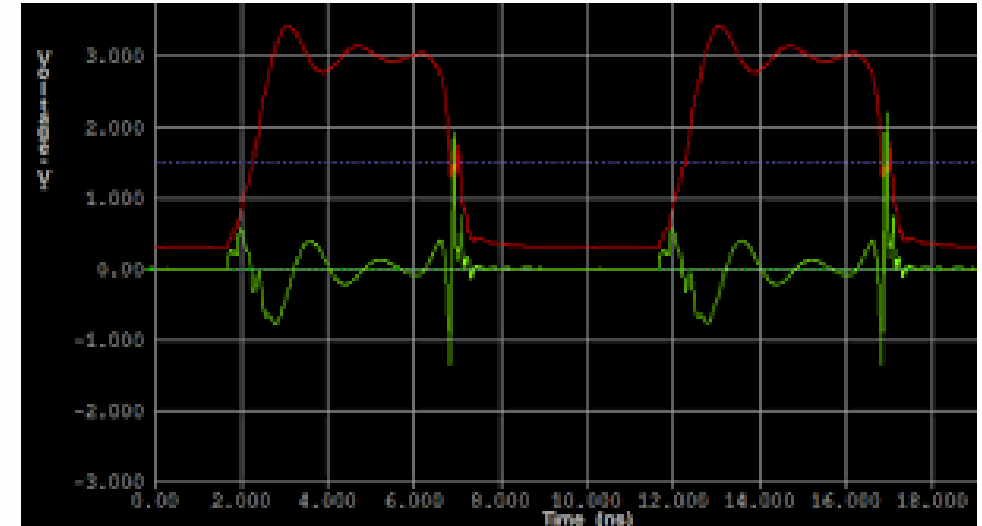


Analysis - Plots and Results (Cont.)

Topology - DDR - CLK



Analysis Result



Analysis Parameters – Requirements

As per SoC,

$$V_{OH} = 1400mV$$

$$V_{OL} = 700mV$$

Both the values are meeting the requirement and the results are **pass**.

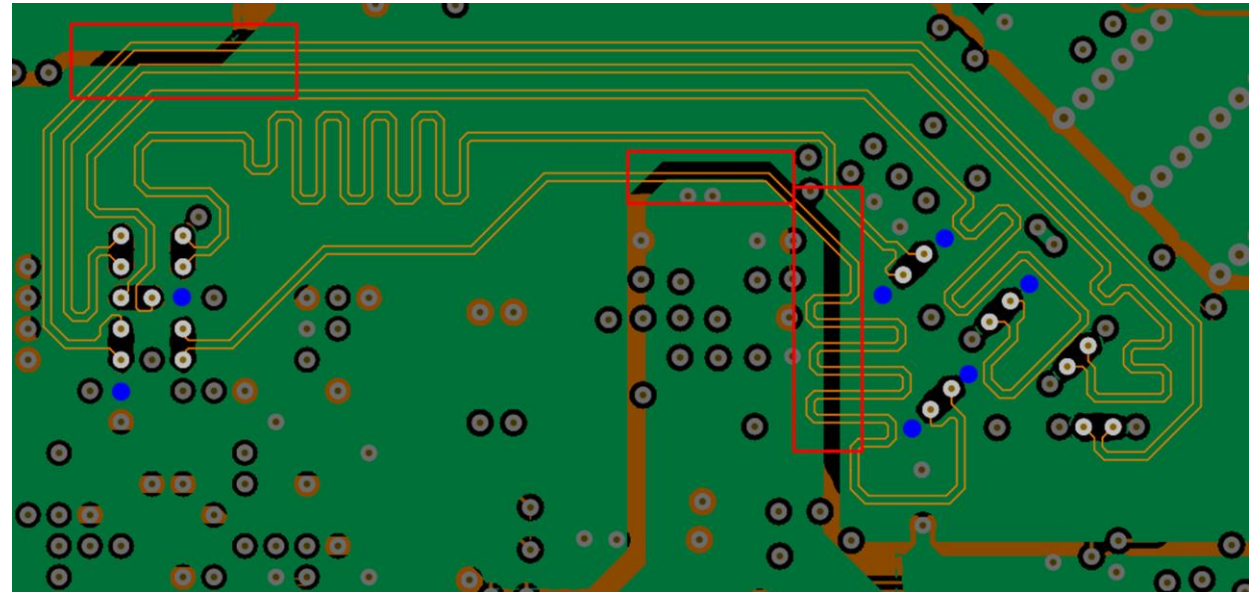


Layout Recommendations (Cont.)

The PCB layout's performance can be increased by the following recommendations

MIPI Signals : DeSerializer to SoC

1. Add **GND** Vias near the Signal Layer Switching Vias.
2. **Layer 3** traces has less spacing with GND polygon.
Need to increase spacing. It should be $5H$ ($5 \times 2.7 = 13.5$ mils)
3. **Layer 3** traces doesn't have the sandwiched solid GND reference plane.
Layer -2 has Solid GND reference. But,
Layer -4 has split planes.



  Place Vias

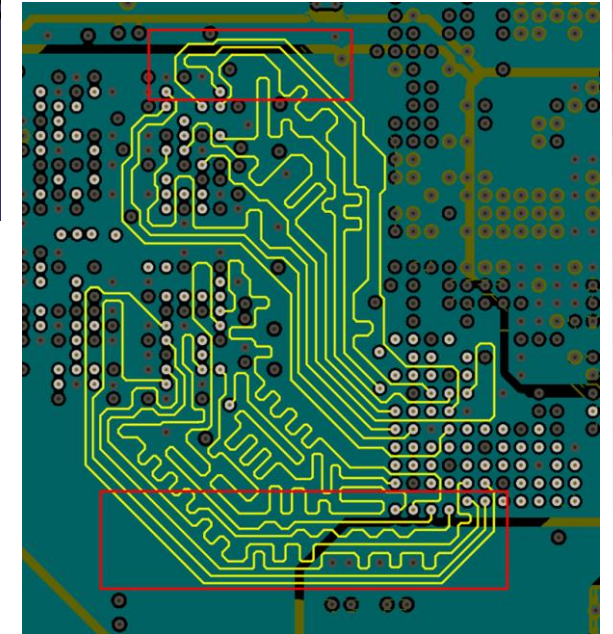
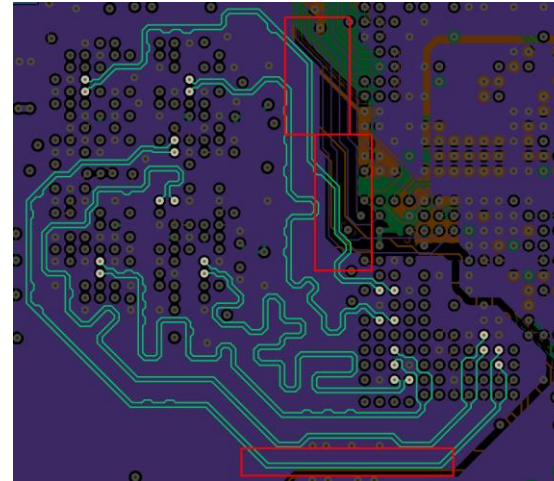


Layout Recommendations

The PCB layout's performance can be increased by the following recommendations

DDR Signals : DDR to SoC

1. **Layer 4** Differential traces has less spacing with GND polygon. Need to increase spacing/Clearance.
2. **Layer 4** traces doesn't have the solid GND reference plane. It has to be one reference plane without any splits. In layer – 5 split GND and other highspeed signal Traces are there.
3. Similar, **Layer 7** single Ended traces doesn't have the solid GND reference plane. It has to be one reference plane without any splits. In **Layer 6** split GND and other highspeed signal Traces are there.



Layout Implementations

Suggested recommendations are incorporated to the PCB layout to enhance its performance.

MIPI Signals : DeSerializer to SoC

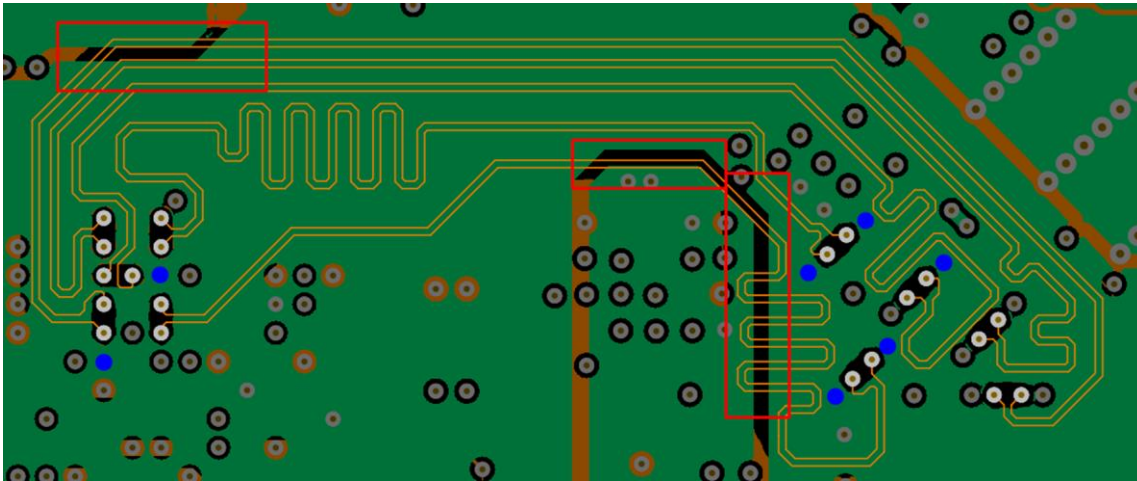
Clearance:

- Routing optimized to increase the spacing (5H - 20 mils) between GND and MIPI signal traces.
- Solid GND reference provided in Layer 4

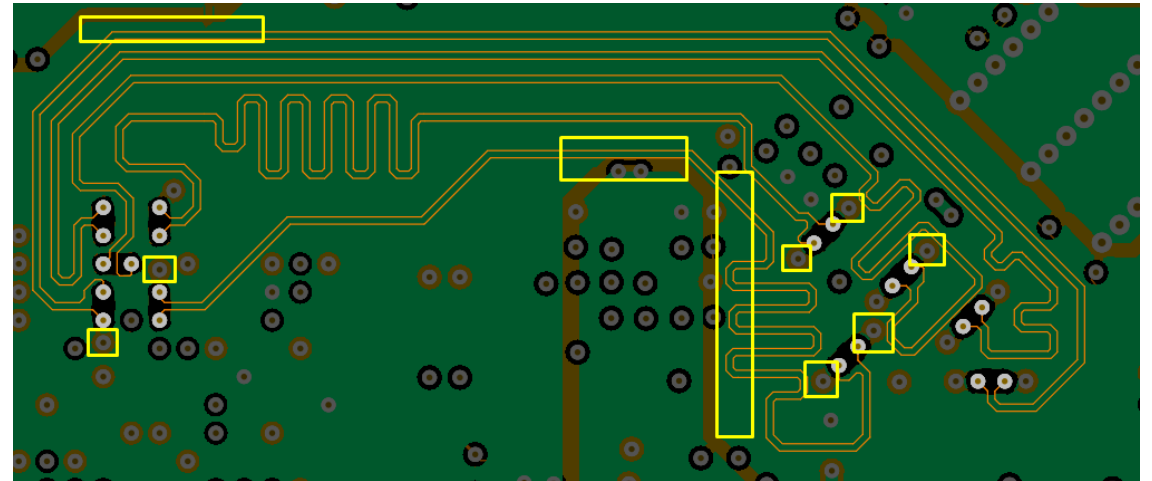
Vias:

Vias placed at the specified locations

Before Analysis



After Analysis



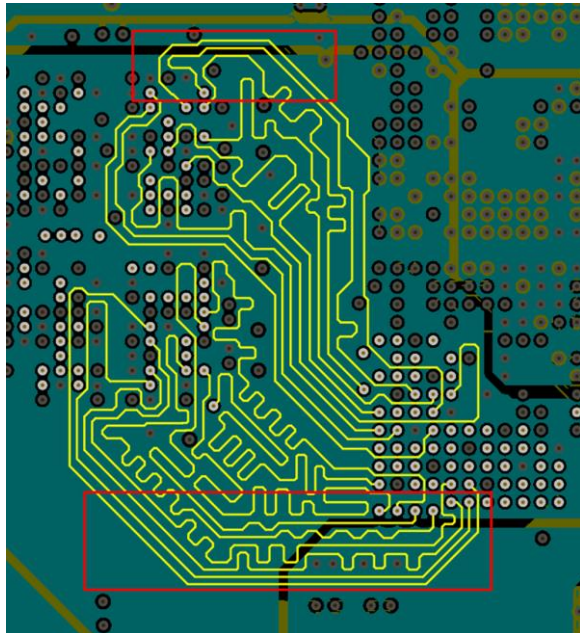
Layout Implementations (Cont.)

DDR Single Ended Signals : DDR to SoC

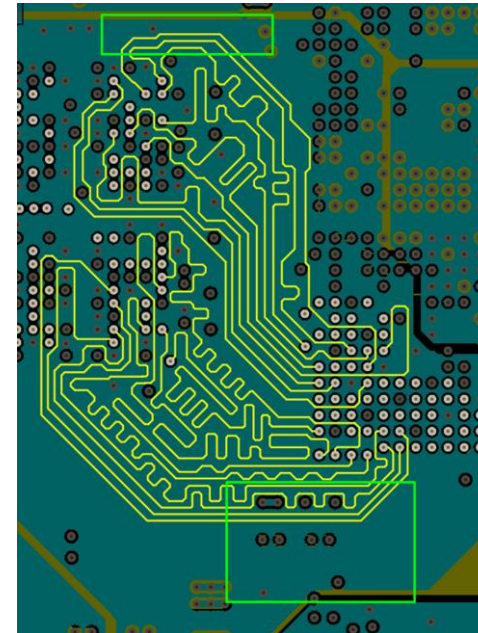
Clearance:

GND Polygon optimized in Layer 6 to providing a solid GND reference for DDR signal traces.

Before Analysis



After Analysis



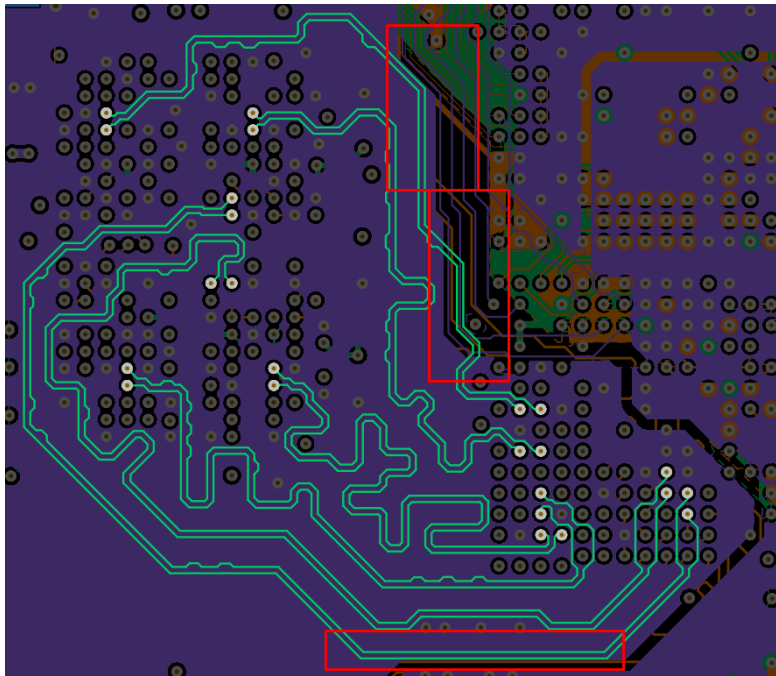
Layout Implementations (Cont.)

DDR Differential Signals : DDR to SoC

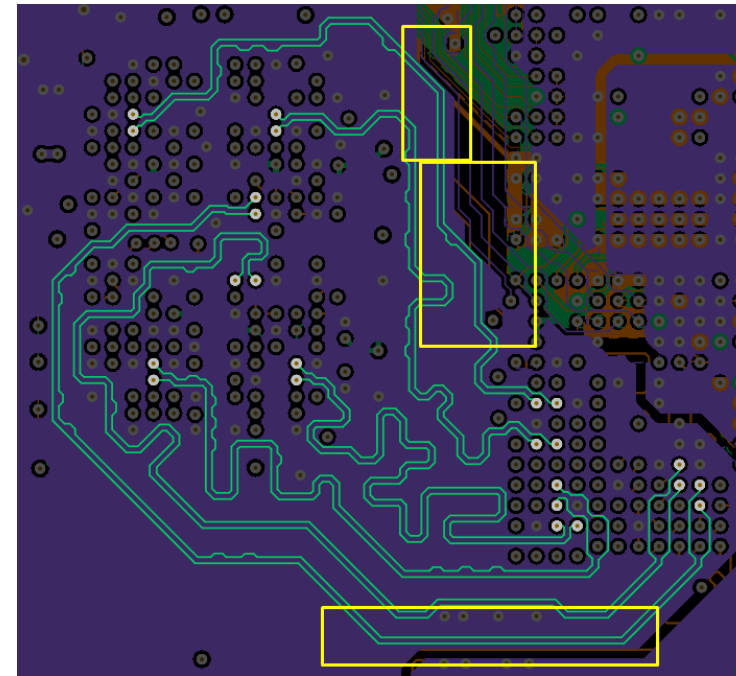
Clearance:

Routing and GND polygons are optimized in Layer 7 for DDR differential signals, providing a solid GND reference for DDR signal traces.

Before Analysis



After Analysis



Customer Testimonial

Excited to present a testimonial from a content client, emphasizing the success and positive impact of our Signal Integrity Analysis.

“Engaging the team for Signal Integrity (SI) Analysis was a game-changer for our project. Their meticulous approach ensured top-notch quality, uncovering potential issues and providing effective solutions. The detailed insights provided during the analysis were invaluable, contributing significantly to the overall success of our project. The cost-effective modifications to copper pours demonstrated their commitment to optimizing resources. Moreover, the timely delivery showcased their efficiency. We are highly satisfied with the quality, and timely delivery of the SI analysis, marking a significant enhancement in the reliability and efficiency of our electronic design!”



Conclusion

We provided the client with a set of recommendations to enhance the performance of the HS signals and made layout design adjustments accordingly. This underscores our dedication to delivering top-notch work and showcasing our technical proficiency.

We go beyond technical considerations, focusing on optimizing layout signals to enhance performance. This involves blending our expertise with a thorough grasp of the client's unique needs.

We are dedicated to providing top-tier analysis services, demonstrating our unmatched skills and unwavering reliability in delivering exceptional results.

