Signal Integrity Analysis

Scope : Enhance Signal Reliability and Optimize Performance

Application : Advanced Driver Assistance Systems

In automotive applications, signal integrity practices are essential for safety and driver-assistance systems. By integrating these practices into PCB layout, signal quality is preserved as it travels from driver components to receivers.

Signal integrity analysis is critical for ADAS application boards, ensuring reliable and accurate performance across various functions. It helps enhance signal quality, reduce distortions, and address challenges like crosstalk and timing issues. This analysis is particularly important for ADAS applications, where precise signal transmission is vital for optimal functionality and safety.

Signal Integrity Analysis - Challenges

The client has asked for a signal integrity analysis of the layout to ensure top performance. Here, we outline the challenges involved in Signal Integrity Analysis.

Challenges

- Cross Talk
- Ground Bounce
- Reflections and Impedance Mismatch
- Skew and Timing
- Signal Termination
- High-Frequency Effects
- Via Impacts
- Power Distribution
- Noise & EMI effects
- Continuous reference planes

Signal Integrity Analysis - SoW

01 **Analyzing High-Speed Signal Groups**
Listing Impedance and Requirements

02 **Analysis -Hyper Lynx**
Essential Parameters Identification

03 **Performance Analysis**
Plot and Outcome Review

04 **Recommendations**
To enhance Performance

05 **Implementations**
Layout Design Modifications

Study of High Speed Signals / Groups

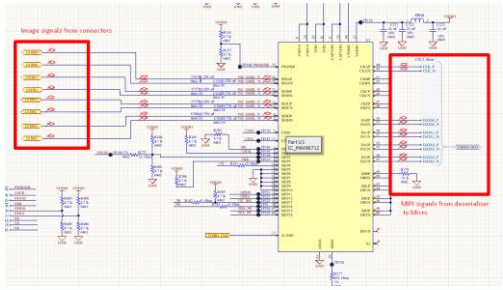
The High Speed Signal circuits in the project are studied thoroughly to evaluate the performance.

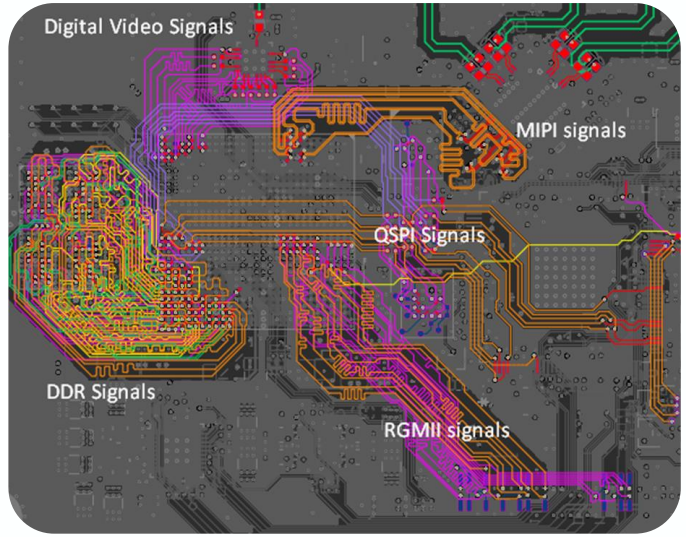
High Speed Signals

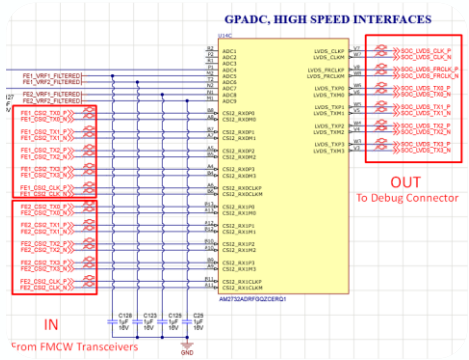
- MIPI - DeSerializer to SoC
- DDR - DDR to SoC
- RGMII - SoC to Debug connector
- DIG_VIDEO – SoC to Serializer
- QSPI – SoC to Flash memory

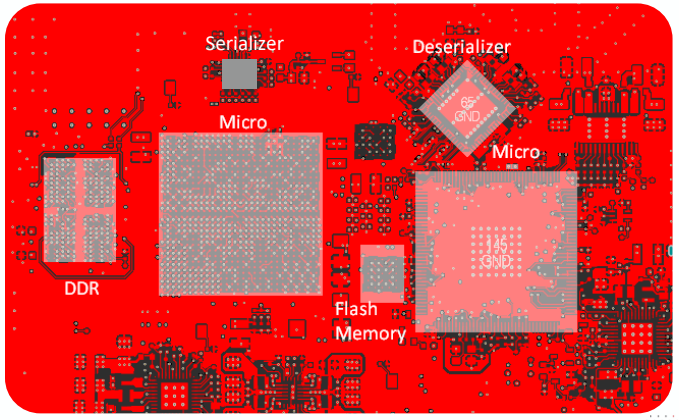
High Speed Signal Circuits

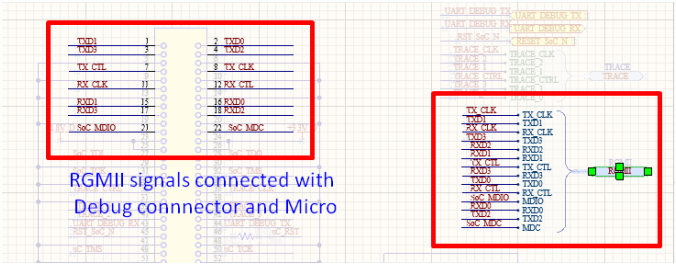
- SoC & DDR.
- Serializer & DeSerializer
- Debug Connector
- Flash memory

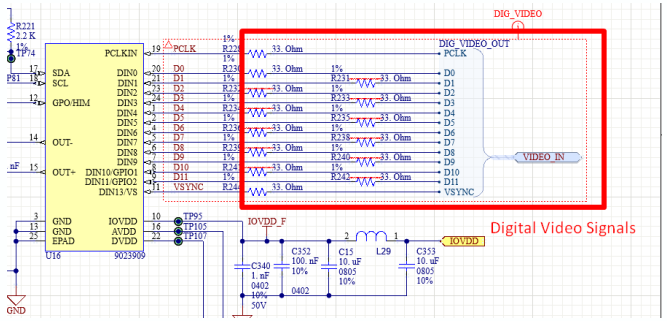








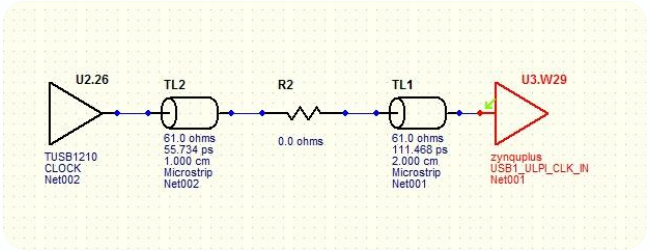


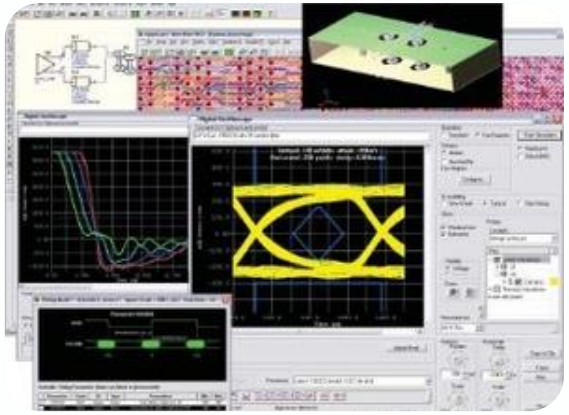


Analysis Execution

We conducted a signal integrity analysis using the **HyperLynx** tool to assess the performance of the layout.

Signal Integrity issues were detected at two levels:

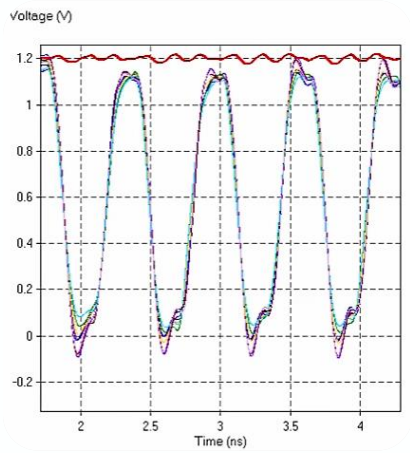


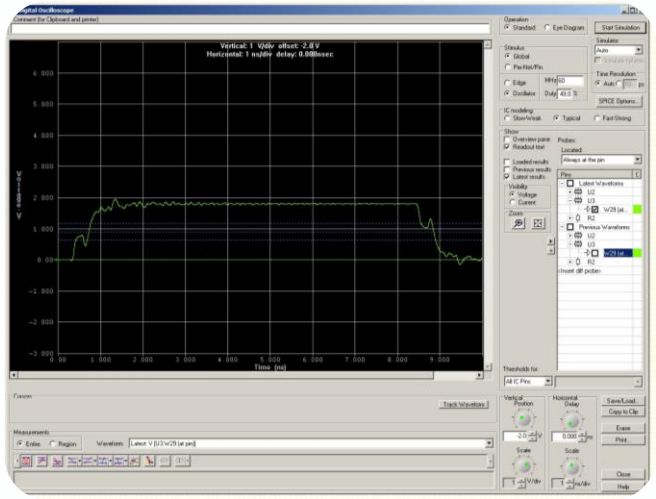


- ➢ Interconnect level and
- ➢ Systems-level

Quantities to calculate include:

- ✓ Impedance Matching.
- ✓ Interactions between the PDN and high-speed signals.
- ✓ Jitter Analysis.
- ✓ Return path discontinuities.
- ✓ Result of Simultaneous Switching Noise (SSN).

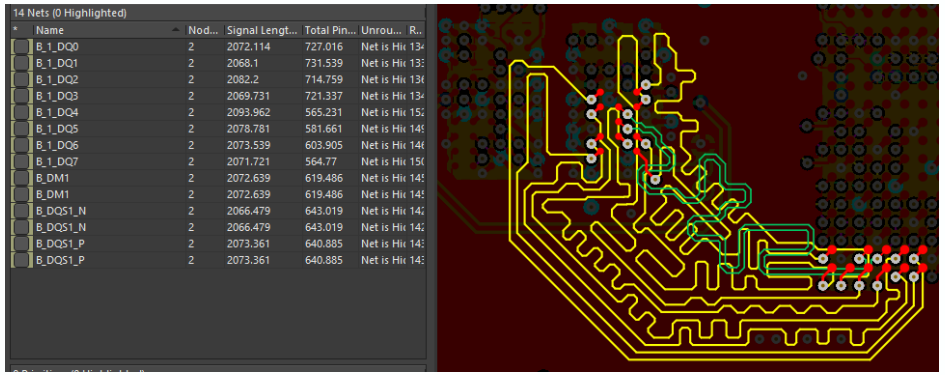


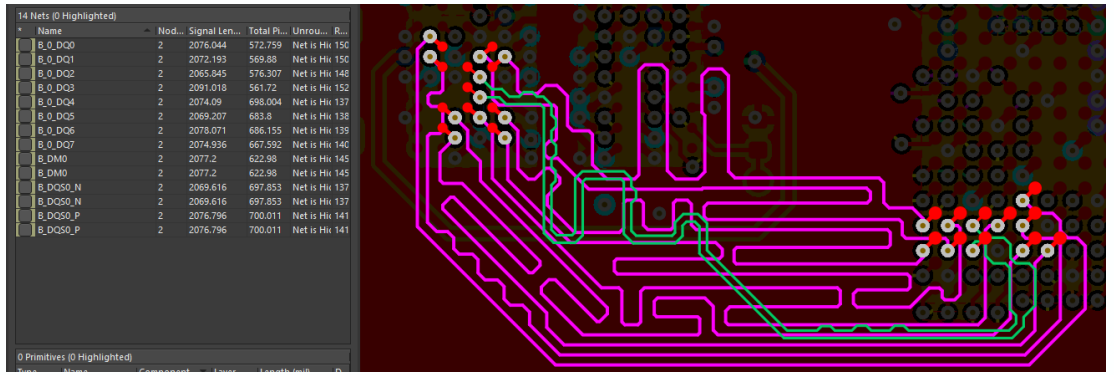


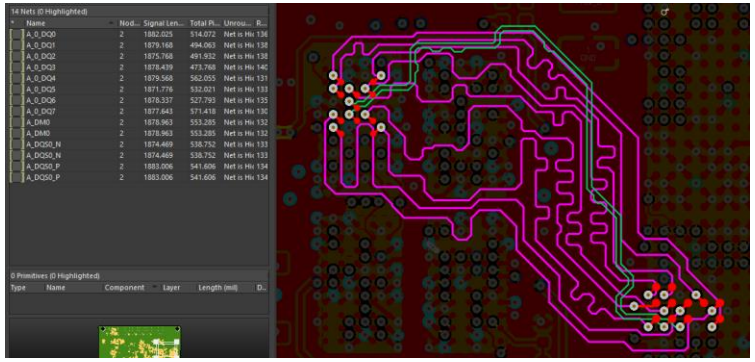
Analysis Execution (Cont.)

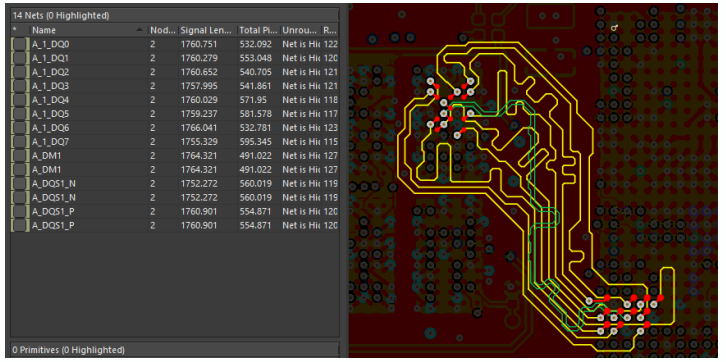
DDR signals – DDR to SoC

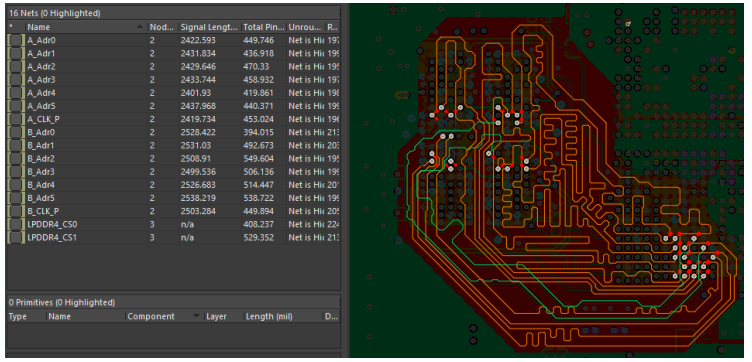
Layout - Routing











CLK and Data's are routed with same trace length(closely)

Analysis Execution (Cont.)

MIPI signals – DeSerializer to SoC

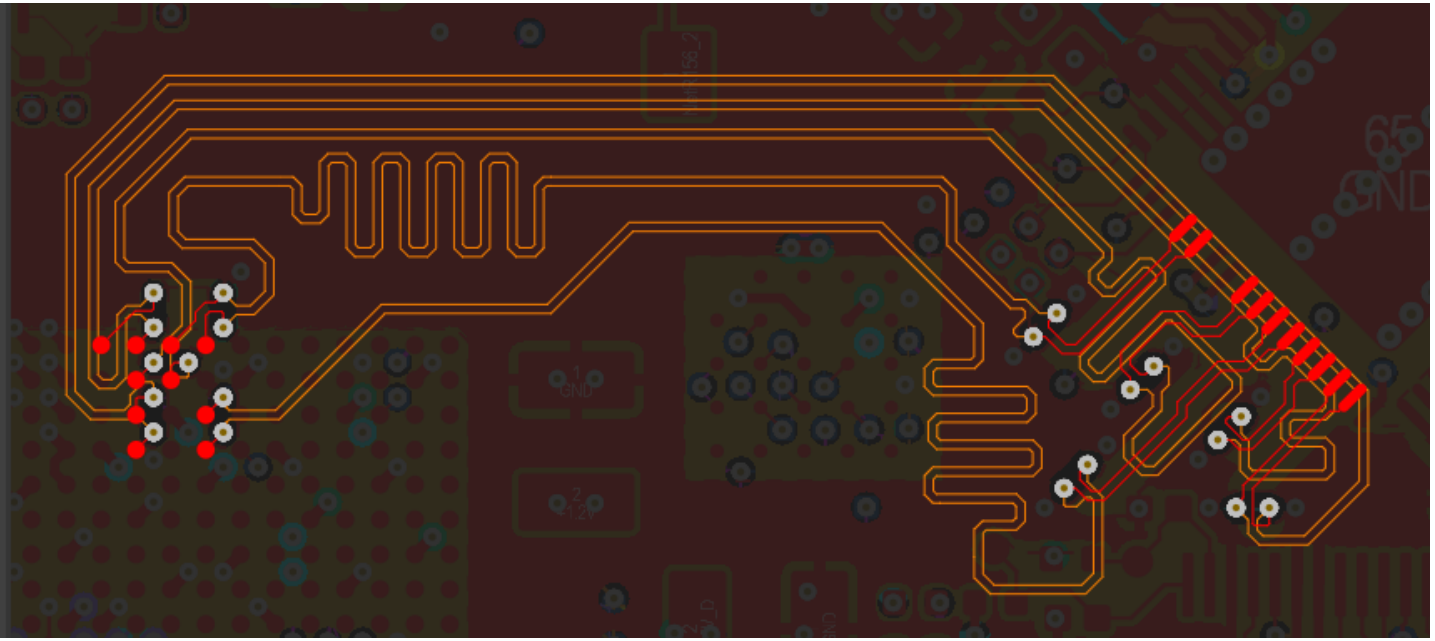
Layout - Routing

Trace Lengths

Layer 3

10 Nets (0 Highlighted)

*	Name	Nod...	Signal Lengt...	Total Pin...	Unrou...	R..
	CAM_MIPI_CLK_N	2	2060	0	Net is Hi	20
	CAM_MIPI_CLK_P	2	2059.475	0	Net is Hi	20
	CAM_MIPI_D0_N	2	2060	0	Net is Hi	20
	CAM_MIPI_D0_P	2	2059.286	0	Net is Hi	20
	CAM_MIPI_D1_N	2	2060	0	Net is Hi	20
	CAM_MIPI_D1_P	2	2059.02	0	Net is Hi	20
	CAM_MIPI_D2_N	2	2060	0	Net is Hi	20
	CAM_MIPI_D2_P	2	2059.215	0	Net is Hi	20
	CAM_MIPI_D3_N	2	2059.078	0	Net is Hi	20
	CAM_MIPI_D3_P	2	2058.006	0	Net is Hi	20

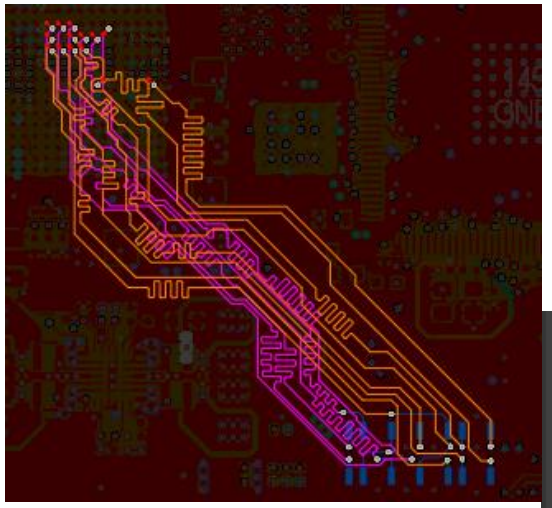


CLK and Data's are routed with same trace length (closely)

Analysis Execution (Cont.)

Layout - Routing

RGMII signals – DeSerializer to SoC



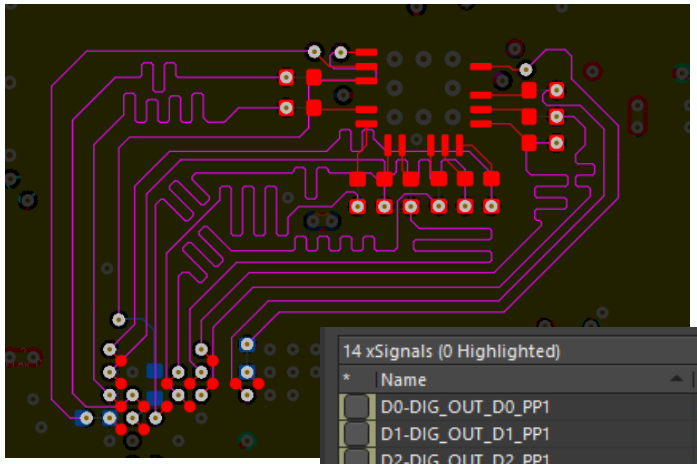
Trace Lengths

14 Nets (0 Highlighted)

*	Name	Nod...	Signal Len...	Total Pi...	Unrou...	R...
	RGMII.MDC	2	2249.999	0	Net is Hi	224
	RGMII.MDIO	2	2249.999	0	Net is Hi	224
	RGMII.RXD0	2	2250.001	0	Net is Hi	225
	RGMII.RXD1	2	2250	0	Net is Hi	224
	RGMII.RXD2	2	2249.999	0	Net is Hi	224
	RGMII.RXD3	2	2250	0	Net is Hi	224
	RGMII.RX_CLK	2	2249.999	0	Net is Hi	224
	RGMII.RX_CTL	2	2249.999	0	Net is Hi	225
	RGMII.TXD0	2	2249.999	0	Net is Hi	225
	RGMII.TXD1	2	2251.025	0	Net is Hi	225
	RGMII.TXD2	2	2250.001	0	Net is Hi	224
	RGMII.TXD3	2	2250.001	0	Net is Hi	224
	RGMII.TX_CLK	2	2249.999	0	Net is Hi	225
	RGMII.TX_CTL	2	2250	0	Net is Hi	224

CLK and Data's are routed with same trace length (closely)

DIG_VIDEO signals – SoC to Serializer



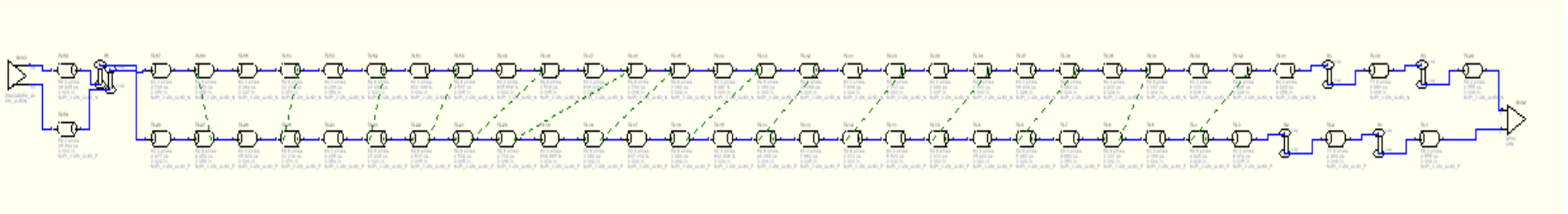
Trace Lengths

14 xSignals (0 Highlighted)

*	Name	Node ...	Signal Length (...	T...	R...	U...
	D0-DIG_OUT_D0_PP1	4	1099.692	0	109	0
	D1-DIG_OUT_D1_PP1	4	1100.001	0	110	0
	D2-DIG_OUT_D2_PP1	4	1102.539	0	110	0
	D3-DIG_OUT_D3_PP1	4	1100.305	0	110	0
	D4-DIG_OUT_D4_PP1	4	1100.001	0	110	0
	D5-DIG_OUT_D5_PP1	4	1100.036	0	110	0
	D6-DIG_OUT_D6_PP1	4	1100.145	0	110	0
	D7-DIG_OUT_D7_PP1	4	1100.267	0	110	0
	D8-DIG_OUT_D8_PP1	4	1100	0	110	0
	D9-DIG_OUT_D9_PP1	4	1100.145	0	110	0
	D10-DIG_OUT_D10_PP1	4	1100.001	0	110	0
	D11-DIG_OUT_D11_PP1	4	1100.107	0	110	0
	PCLK-DIG_OUT_PCLK_PP1	4	1101.372	0	110	0
	VSYNC-DIG_OUT_VSYNC_PP1	4	1100.153	0	110	0

Analysis - Plots and Results

Topology – MIPI-CLK



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 740mV

VinL = 550mV

High Speed Mode:

VinH = 460mV

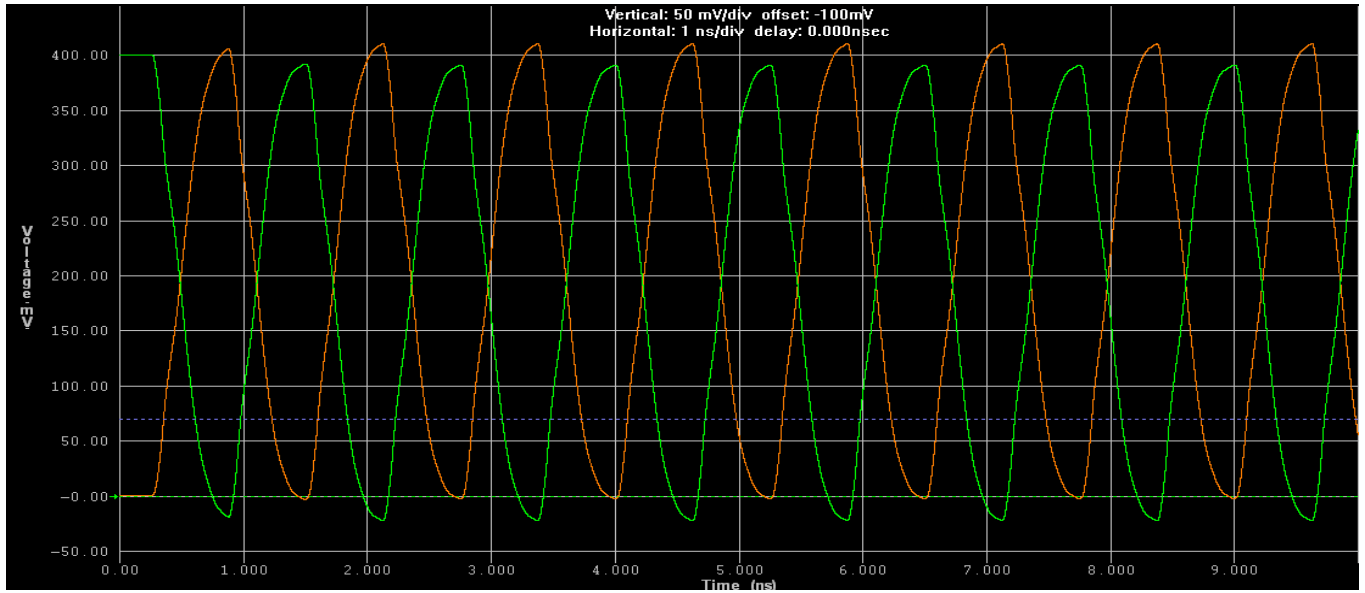
VinL = 40mV

MIPI interface standard requirements

VinH = 235mV

VinL = 165mV

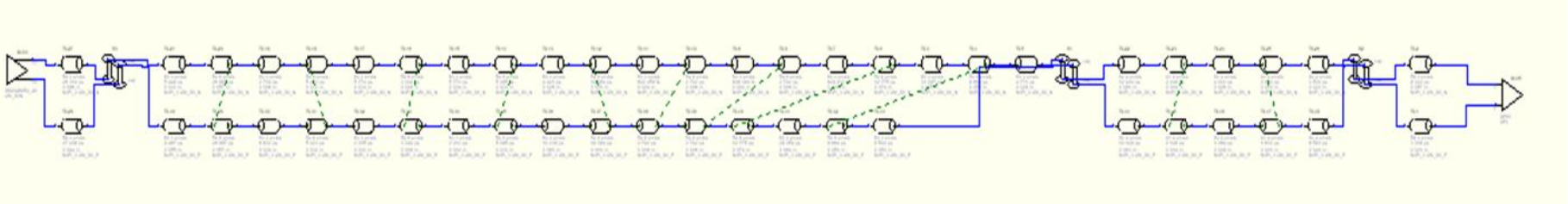
Analysis Result



Both values meet the requirements, resulting in a **pass**.

Analysis - Plots and Results (Cont.)

Topology - MIPI - DATA



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 700mV

VinL = 500mV

High Speed Mode:

VinH = 300V

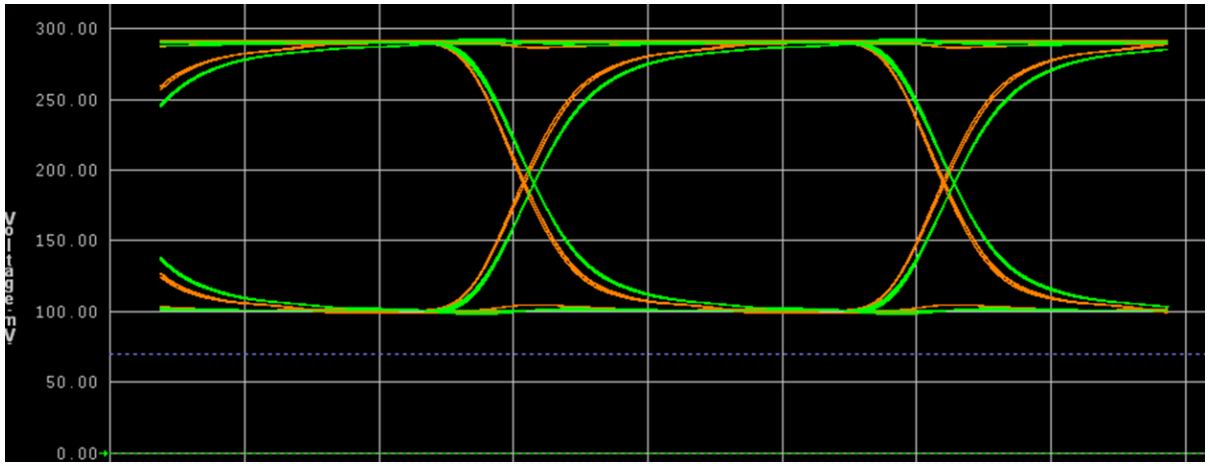
VinL = 60mV

MIPI interface standard requirements

VinH = 205mV

VinL = 145mV

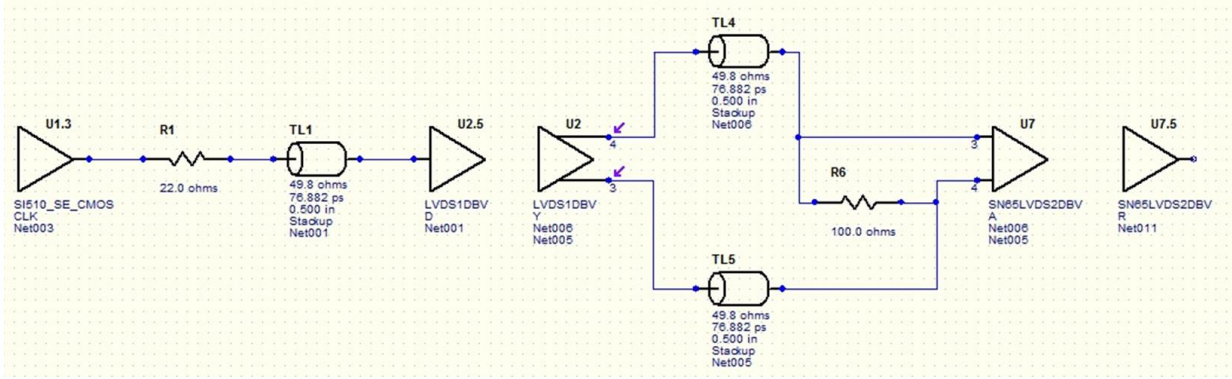
Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Analysis - Plots and Results (Cont.)

Topology - DDR - CLK



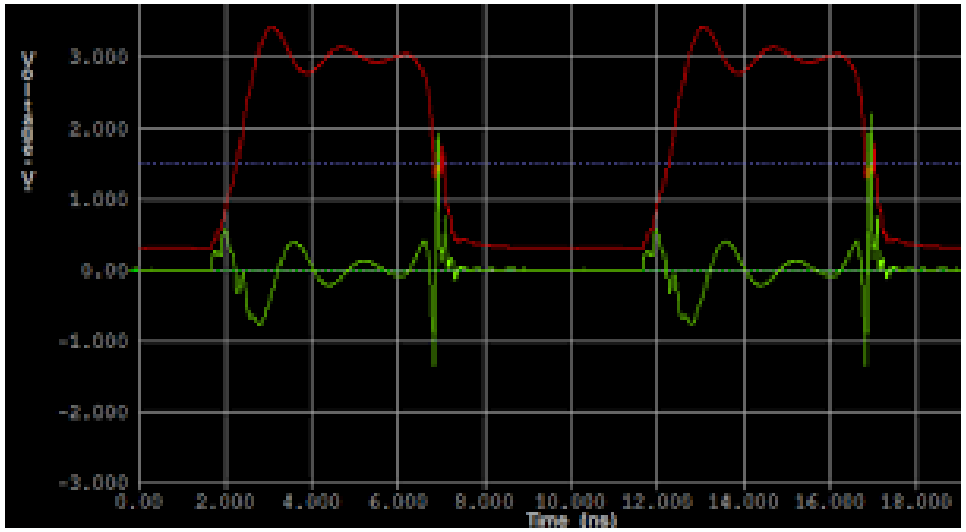
Analysis Parameters – Requirements

As per SoC,

V_{OH} = 1400mV

V_{OL} = 700mV

Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Layout Recommendations (Cont.)

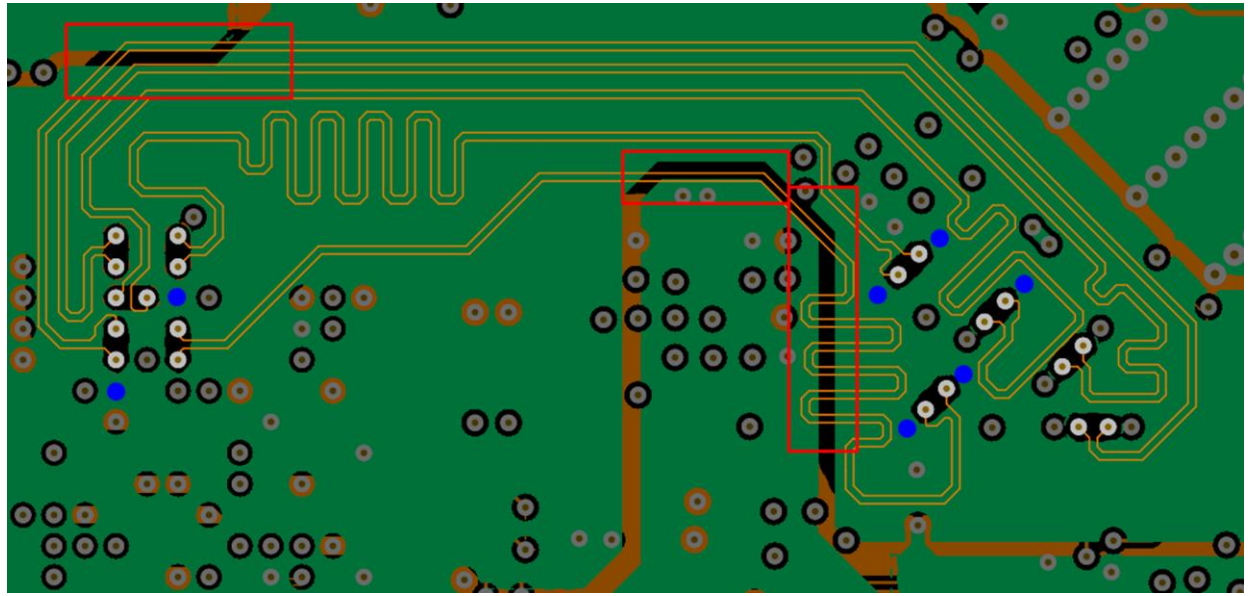
The PCB layout's performance can be increased by the following recommendations

MIPI Signals : DeSerializer to SoC

1. Add **GND** Vias near the Signal Layer Switching Vias.

2. **Layer 3** traces has less spacing with GND polygon.
Need to increase spacing. It should be
5H (5 x 2.7= 13.5 mils)

3. **Layer 3** traces doesn't have the sandwiched solid GND reference plane.
Layer -2 has Solid GND reference. But,
Layer -4 has split planes.



Place Vias

Layout Recommendations

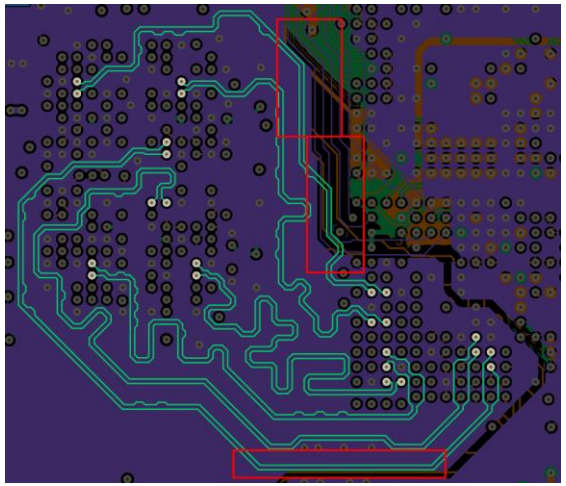
The PCB layout's performance can be increased by the following recommendations

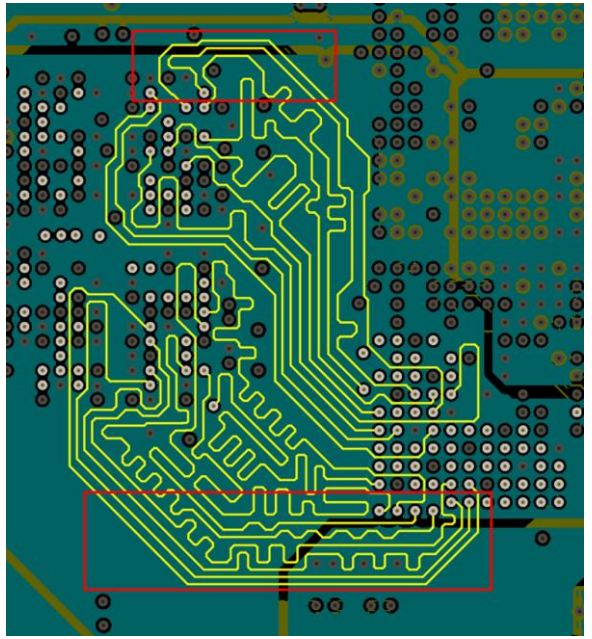
DDR Signals : DDR to SoC

1. **Layer 4** Differential traces has less spacing with GND polygon. Need to increase spacing/Clearance.

2. **Layer 4** traces doesn't have the solid GND reference plane. It has to be one reference plane without any splits.
In layer – 5 split GND and other highspeed signal Traces are there.

3. Similar, Layer 7 single Ended traces doesn't have the solid GND reference plane. It has to be one reference plane without any splits.
In Layer 6 split GND and other highspeed signal Traces are there.





Layout Implementations

Suggested recommendations are incorporated to the PCB layout to enhance its performance.

MIPI Signals : DeSerializer to SoC

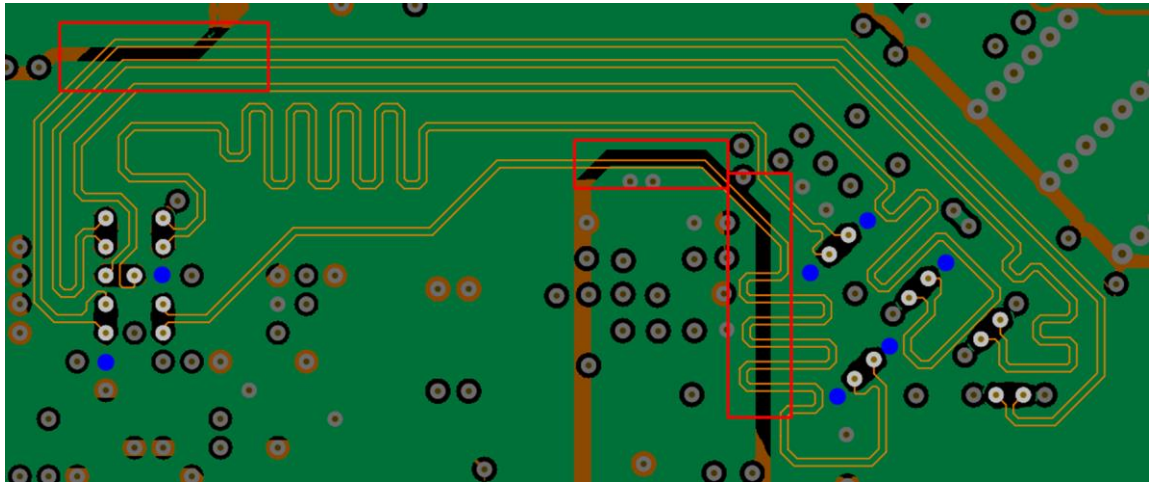
Clearance:

- Routing optimized to increase the spacing (5H - 20 mils) between GND and MIPI signal traces.
- Solid GND reference provided in Layer 4

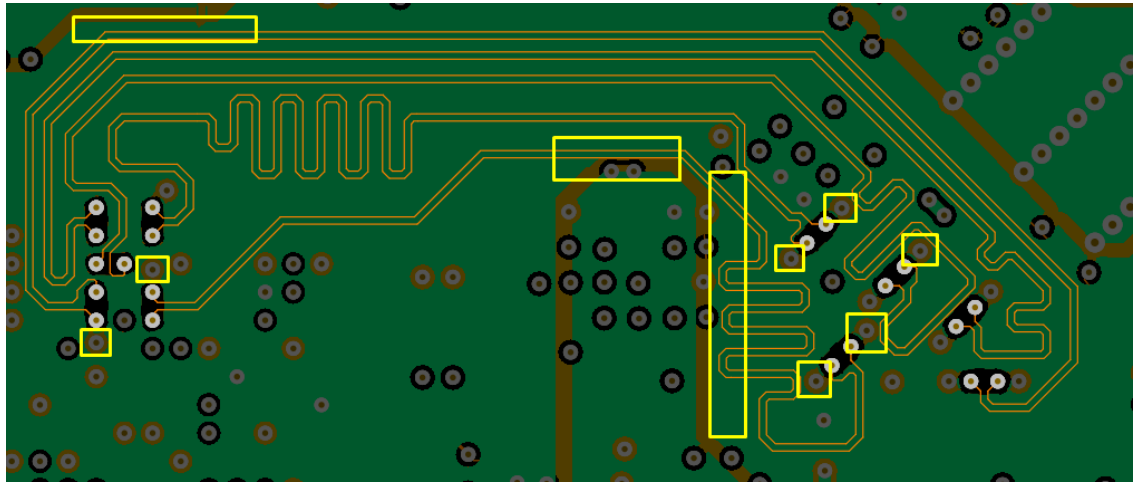
Vias:

Vias placed at the specified locations

Before Analysis



After Analysis



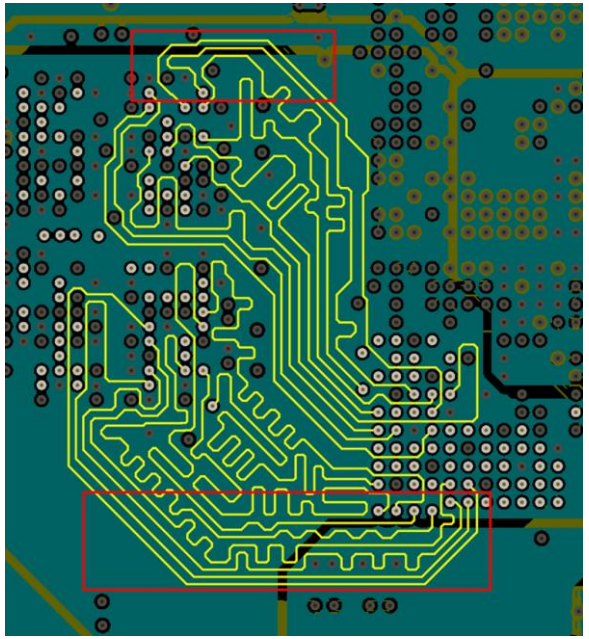
Layout Implementations (Cont.)

DDR Single Ended Signals : DDR to SoC

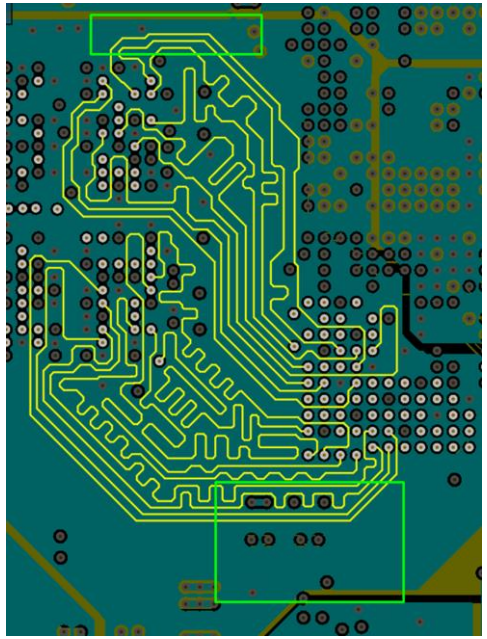
Clearance:

GND Polygon optimized in Layer 6 to providing a solid GND reference for DDR signal traces.

Before Analysis



After Analysis



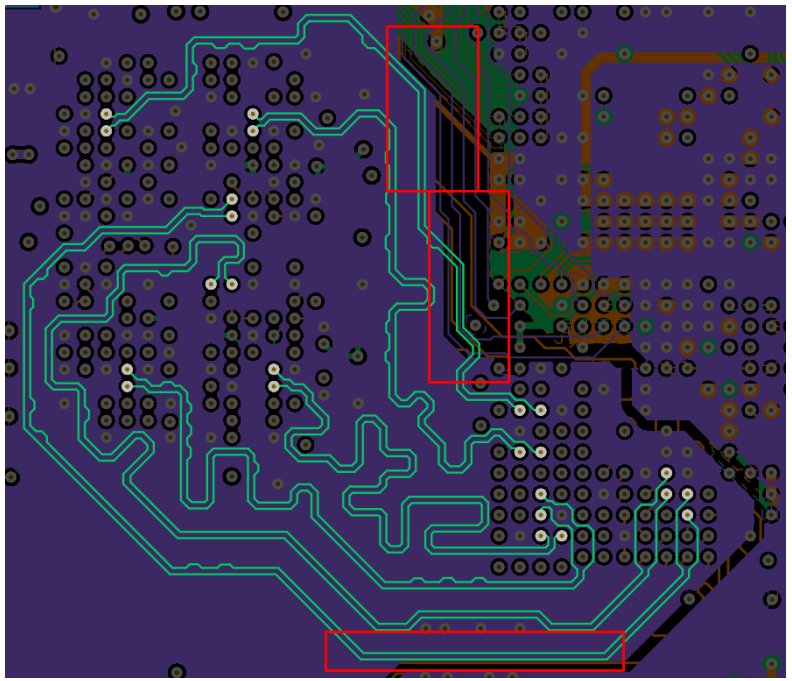
Layout Implementations (Cont.)

DDR Differential Signals : DDR to SoC

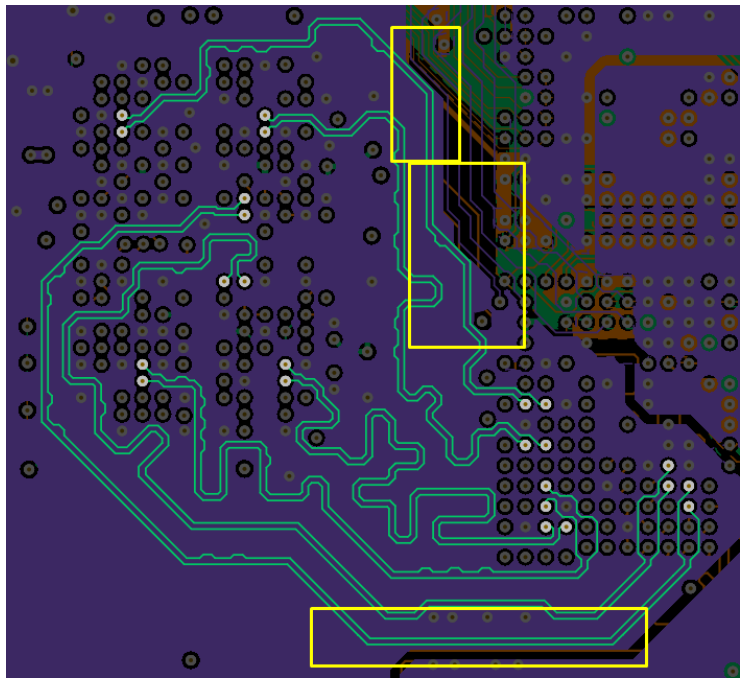
Clearance:

Routing and GND polygons are optimized in Layer 7 for DDR differential signals, providing a solid GND reference for DDR signal traces.

Before Analysis



After Analysis



Customer Testimonial

Excited to present a testimonial from a content client, emphasizing the success and positive impact of our Signal Integrity Analysis.

"Engaging the team for Signal Integrity (SI) Analysis was a game-changer for our project. Their meticulous approach ensured top-notch quality, uncovering potential issues and providing effective solutions. The detailed insights provided during the analysis were invaluable, contributing significantly to the overall success of our project. The cost-effective modifications to copper pours demonstrated their commitment to optimizing resources. Moreover, the timely delivery showcased their efficiency. We are highly satisfied with the quality, and timely delivery of the SI analysis, marking a significant enhancement in the reliability and efficiency of our electronic design!"

Conclusion

We provided the client with a set of recommendations to enhance the performance of the HS signals and made layout design adjustments accordingly. This underscores our dedication to delivering top-notch work and showcasing our technical proficiency.

We go beyond technical considerations, focusing on optimizing layout signals to enhance performance. This involves blending our expertise with a thorough grasp of the client's unique needs.

We are dedicated to providing top-tier analysis services, demonstrating our unmatched skills and unwavering reliability in delivering exceptional results.