Signal Integrity Analysis
Cascaded Radar Sensor Module

Scope : Ensure Reliable Signal Transmission & Optimize Performance

Application : ADAS – Enhanced Performance

In the automotive field, the Cascaded Radar Sensor Module finds application in various safety and driver-assistance systems. Incorporating Signal integrity practices into PCB layout ensures the preservation of signal quality as it travels from a driver component to a receiver.

Signal integrity analysis in a cascaded radar module is crucial for several applications, ensuring reliable and accurate performance. It plays a key role in enhancing signal quality, minimizing distortions, and addressing challenges like crosstalk and timing issues. This analysis is integral for applications such as ADAS, where precise signal transmission is essential for optimal functionality and safety.

Signal Integrity Analysis - Challenges

The client requested to perform signal integrity analysis of the layout to ensure optimal performance. The following outlines the challenges associated with Signal Integrity Analysis.

Challenges

- Reflections and Impedance Mismatch
- Cross Talk
- Skew and Timing
- Ground Bounce
- Signal Termination
- Via Impacts
- Power Distribution
- Noise & EMI effects
- High-Frequency Effects
- Continuous reference planes

Signal Integrity Analysis - SoW

05 **Implementations**
Modifications in Layout design

04 **Recommendations**
To enhance Performance

03 **Analysis – Performance Evaluation**
Plots and Results

02 **Analysis – HyperLynx**
Required Parameters for analysis

01 **Study of High Speed Signals/Groups**
Impedance and Requirements listing

Study of High Speed Signals / Groups

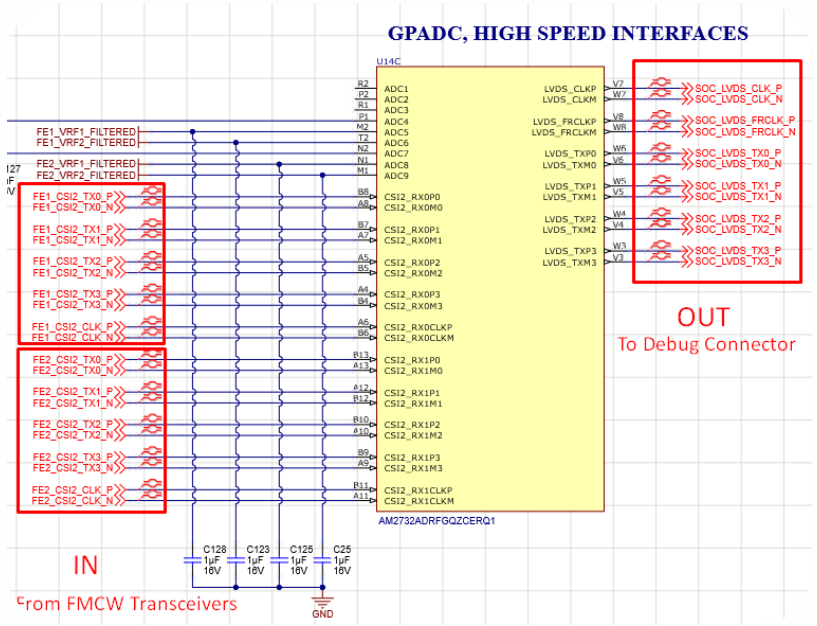
The High Speed Signal circuits in the project are studied thoroughly to evaluate the performance.

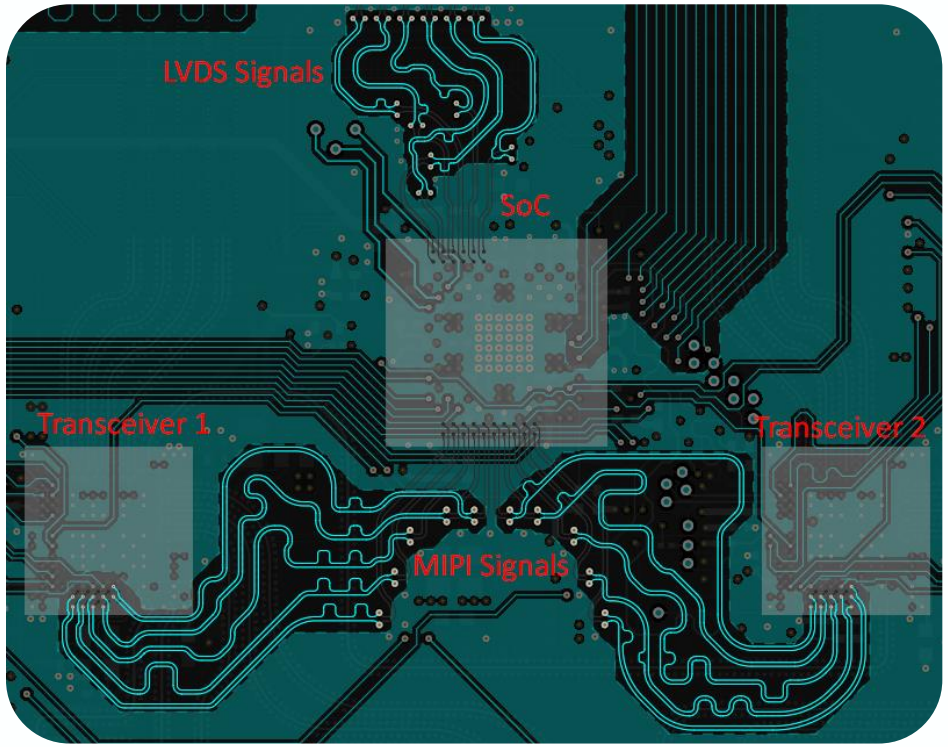
High Speed Signals

- MIPI_1 – FMCW Transceiver_1 to SoC
- MIPI_2 - FMCW Transceiver_2 to SoC
- LVDS – SoC to Debug connector

High Speed Signal Circuits

- FMCW Transceivers
- SoC
- Debug Connector





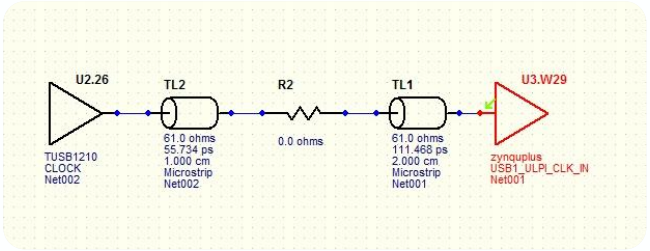
Analysis Execution

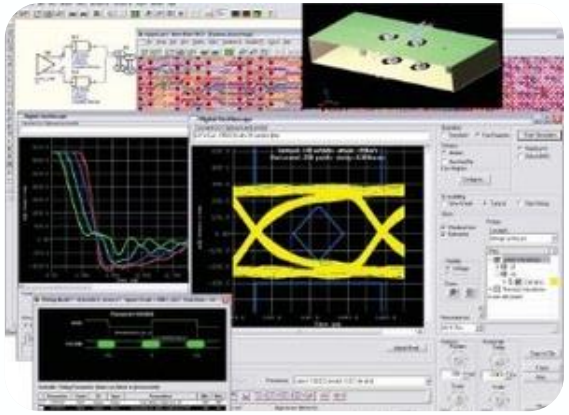
We executed the analysis in **HyperLynx** tool, to evaluate the signal integrity performance of the layout.

Problems of Signal Integrity is identified from two levels:

Interconnect level and

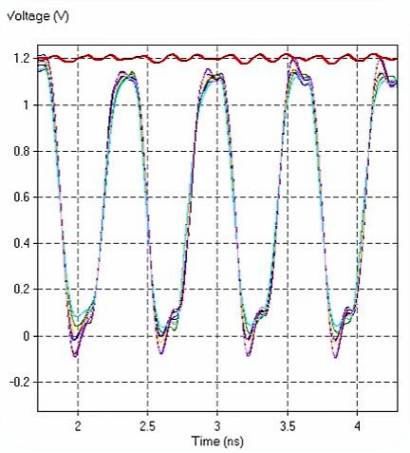
Systems-level

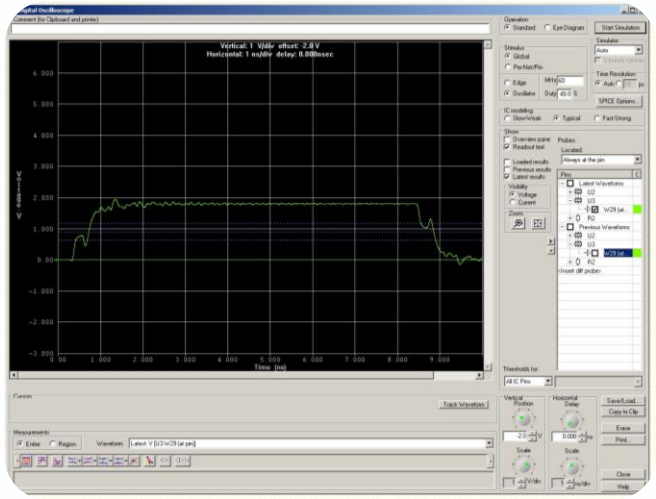




Quantities to calculate include:

- ✓ Impedance Matching.
- ✓ Interactions between the PDN and high-speed signals.
- ✓ Jitter Analysis.
- ✓ Return path discontinuities.
- ✓ Result of Simultaneous Switching Noise (SSN).

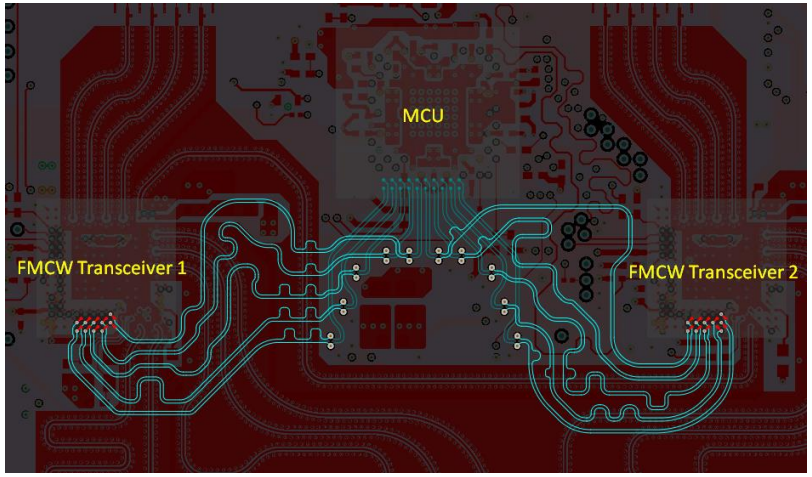




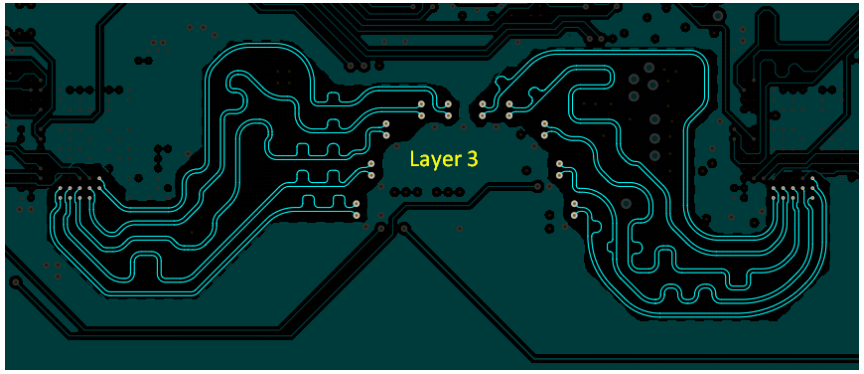
Analysis Execution (Cont.)

MIPI signals – FMCW Transceivers to MCU.

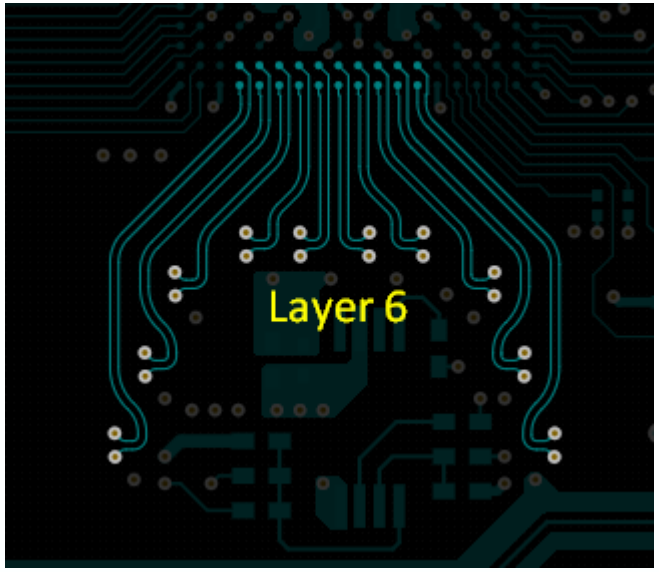
Layout - Routing



Layer 3



Layer 6 (Bottom)



Trace Lengths

Name	Node ...	Signal ...	Total P...	Routed ...	Unr...
FE1_CSI2_CLK_N (-)	2	1780.308	0	1780.523	0
FE1_CSI2_CLK_P (+)	2	1780.817	0	1780.833	0
FE1_CSI2_TX0_N (-)	2	1780.489	0	1780.506	0
FE1_CSI2_TX0_P (+)	2	1780.805	0	1780.809	0
FE1_CSI2_TX1_N (-)	2	1779.957	0	1780.162	0
FE1_CSI2_TX1_P (+)	2	1780.698	0	1780.702	0
FE1_CSI2_TX2_N (-)	2	1780.428	0	1780.636	0
FE1_CSI2_TX2_P (+)	2	1780.471	0	1780.486	0
FE1_CSI2_TX3_N (-)	2	1779.95	0	1780.155	0
FE1_CSI2_TX3_P (+)	2	1780.536	0	1780.54	0

Name	Node ...	Signal ...	Total P...	Routed ...	Unr...
FE2_CSI2_CLK_N (-)	2	1780.125	0	1780.407	0
FE2_CSI2_CLK_P (+)	2	1780.338	0	1780.416	0
FE2_CSI2_TX0_N (-)	2	1780.059	0	1780.064	0
FE2_CSI2_TX0_P (+)	2	1780.396	0	1780.386	0
FE2_CSI2_TX1_N (-)	2	1779.918	0	1780.141	0
FE2_CSI2_TX1_P (+)	2	1780.815	0	1780.828	0
FE2_CSI2_TX2_N (-)	2	1780.847	0	1781.055	0
FE2_CSI2_TX2_P (+)	2	1780.71	0	1780.752	0
FE2_CSI2_TX3_N (-)	2	1780.099	0	1780.295	0
FE2_CSI2_TX3_P (+)	2	1780.687	0	1780.711	0

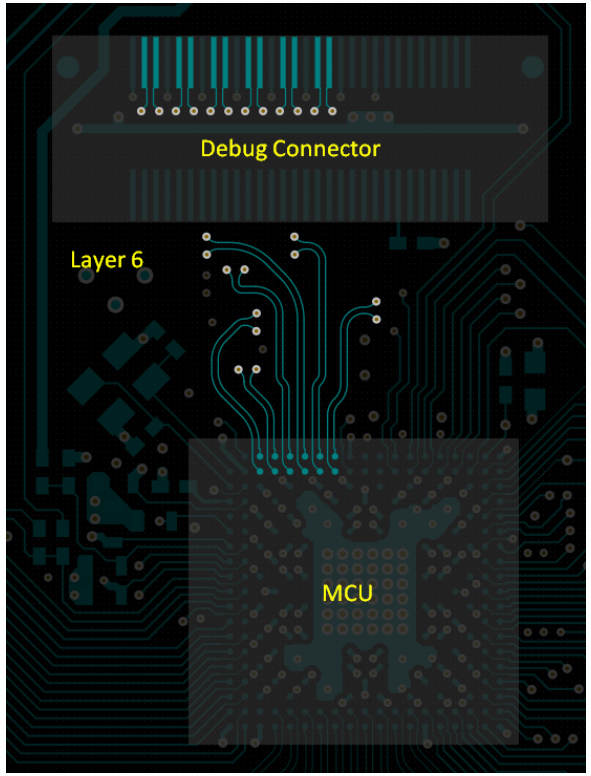
CLK and Data's are routed with same trace length (closely)

Analysis Execution (Cont.)

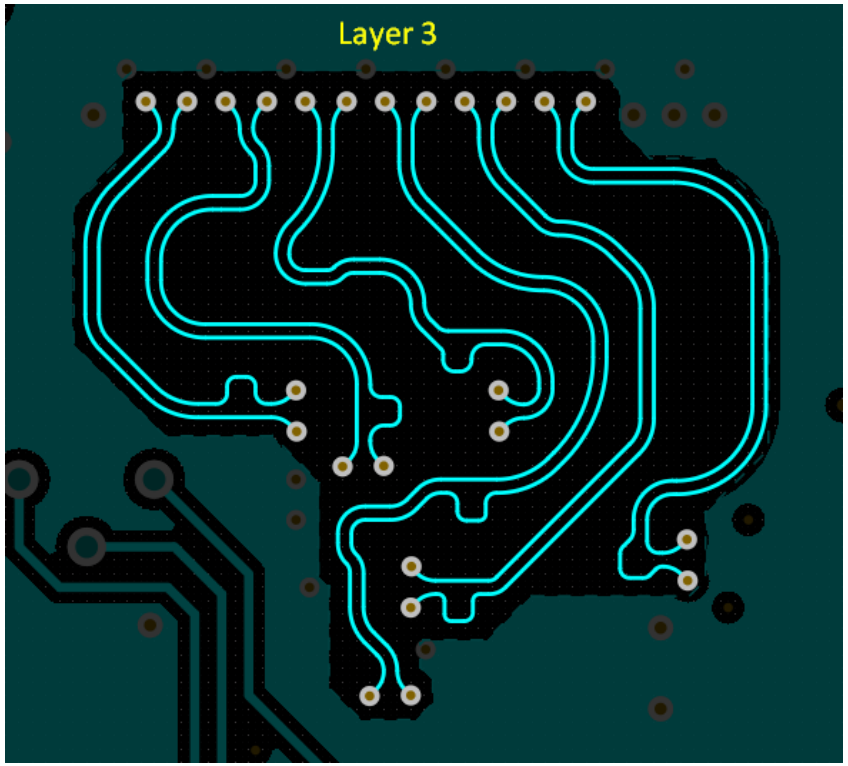
LVDS signals – MCU to Debug Connector.

Layout - Routing

Layer 6 (Bottom)



Layer 3



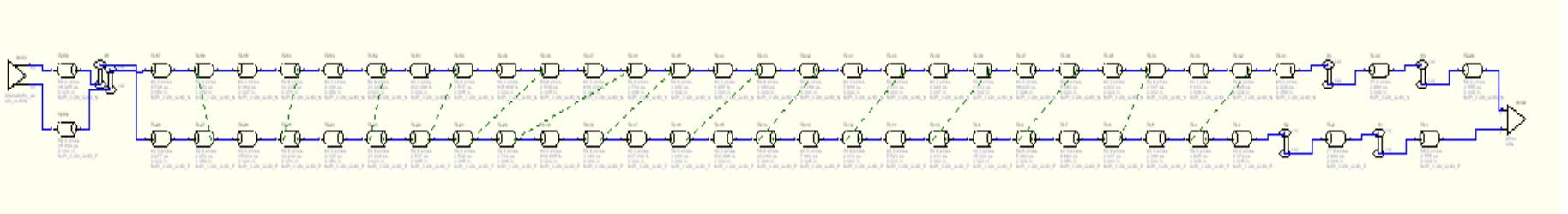
Trace Lengths

Name	Node ...	Signal ...	Total P...	Routed ...	Unr...
SOC_LVDS_CLK_N (-)	2	1033.783	0	1035.461	0
SOC_LVDS_CLK_P (+)	2	1034.159	0	1035.778	0
SOC_LVDS_FRCLK_N (-)	2	1034.513	0	1036.094	0
SOC_LVDS_FRCLK_P (+)	2	1034.252	0	1035.87	0
SOC_LVDS_TX0_N (-)	2	1034.626	0	1036.193	0
SOC_LVDS_TX0_P (+)	2	1033.92	0	1035.552	0
SOC_LVDS_TX1_N (-)	2	1033.809	0	1035.377	0
SOC_LVDS_TX1_P (+)	2	1034.349	0	1035.967	0
SOC_LVDS_TX2_N (-)	2	1033.87	0	1035.444	0
SOC_LVDS_TX2_P (+)	2	1033.832	0	1035.471	0
SOC_LVDS_TX3_N (-)	2	1034.649	0	1036.141	0
SOC_LVDS_TX3_P (+)	2	1034.35	0	1035.98	0

CLK and Data's are routed with same trace length (closely)

Analysis - Plots and Results

Topology - CSI - CLK



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 740mV

VinL = 550mV

High Speed Mode:

VinH = 460mV

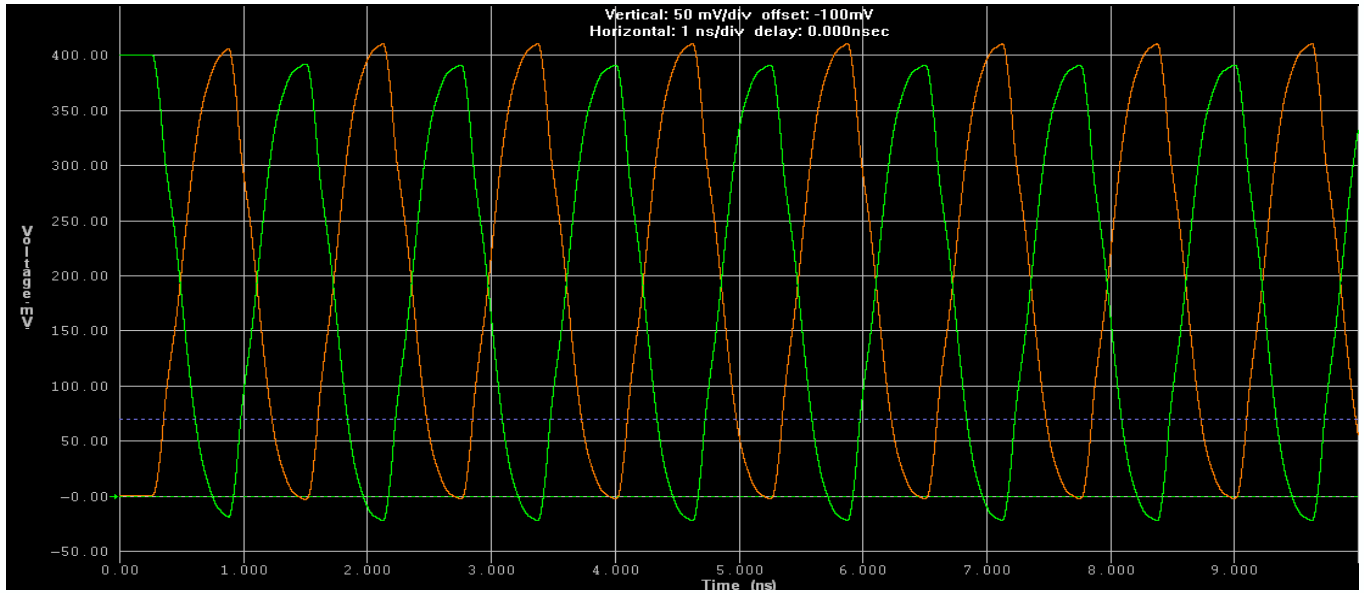
VinL = 40mV

MIPI CSI 2 interface standard requirements

VinH = 235mV

VinL = 165mV

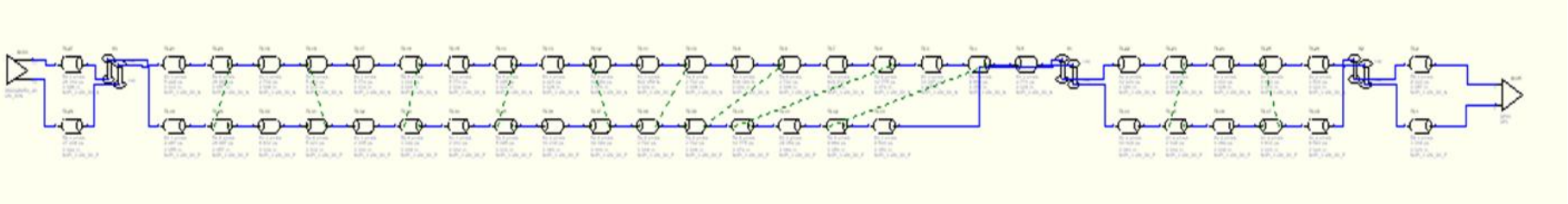
Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Analysis - Plots and Results (Cont.)

Topology - CSI - DATA



Analysis Parameters – Requirements

As per SoC,

Low Power Mode:

VinH = 740mV

VinL = 550mV

High Speed Mode:

VinH = 460mV

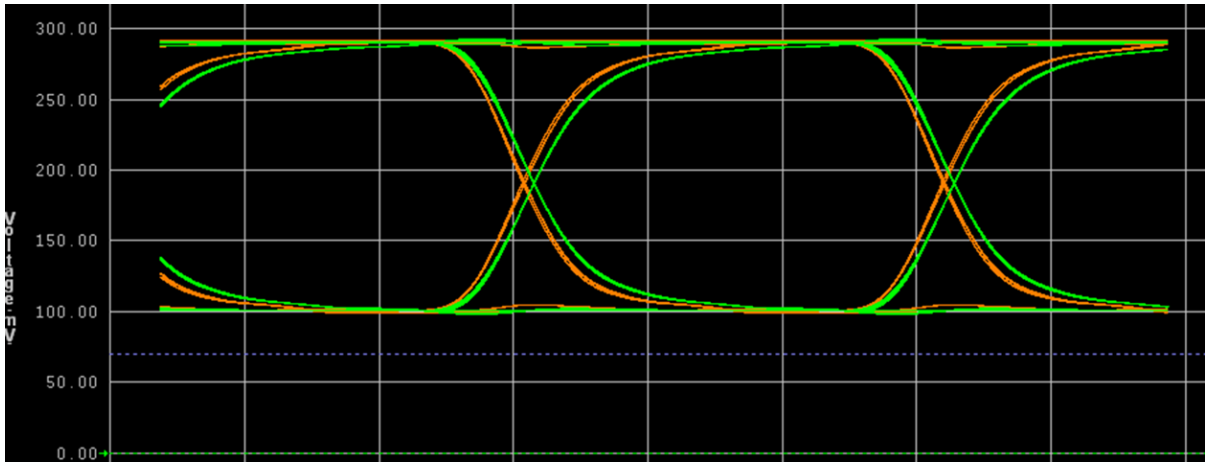
VinL = 40mV

MIPI CSI 2 interface standard requirements

VinH = 235mV

VinL = 165mV

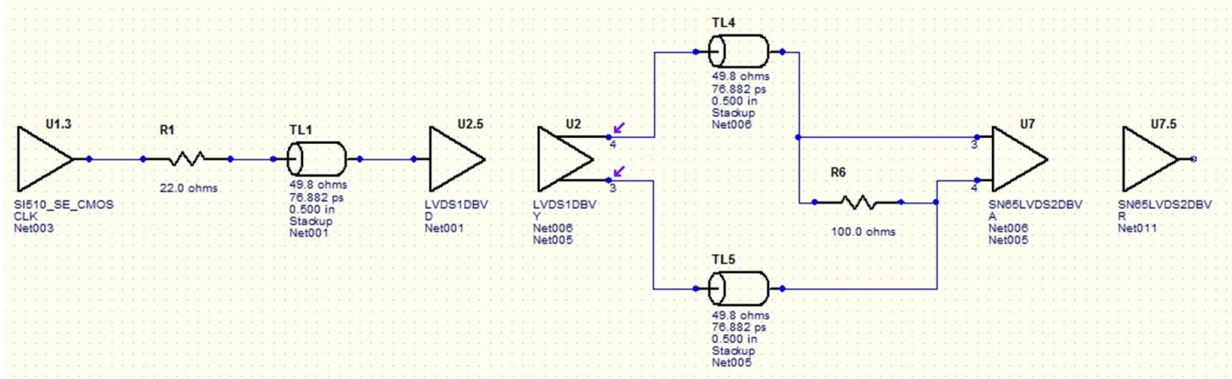
Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Analysis - Plots and Results (Cont.)

Topology - LVDS - CLK



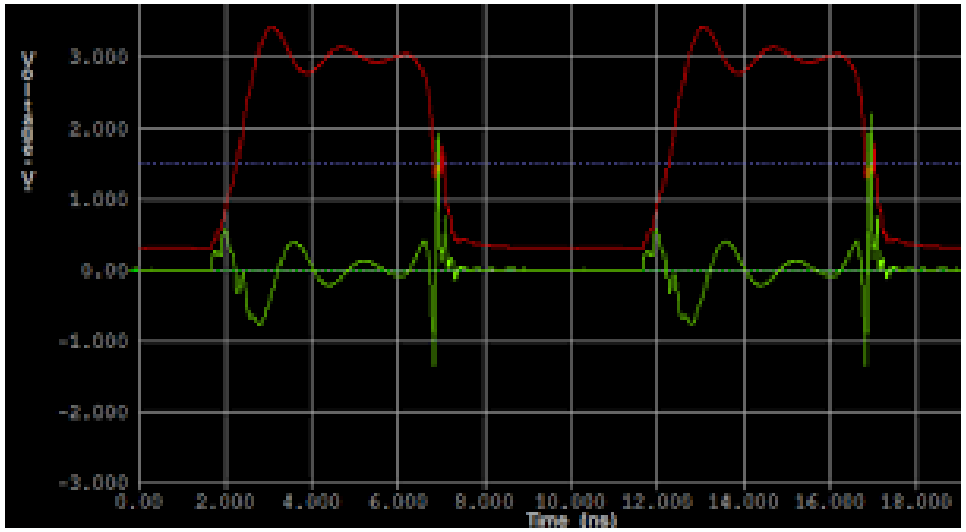
Analysis Parameters – Requirements

As per SoC,

V_{OH} = 1500mV

V_{OL} = 900mV

Analysis Result



Both the values are meeting the requirement and the results are **pass.**

Layout Recommendations (Cont.)

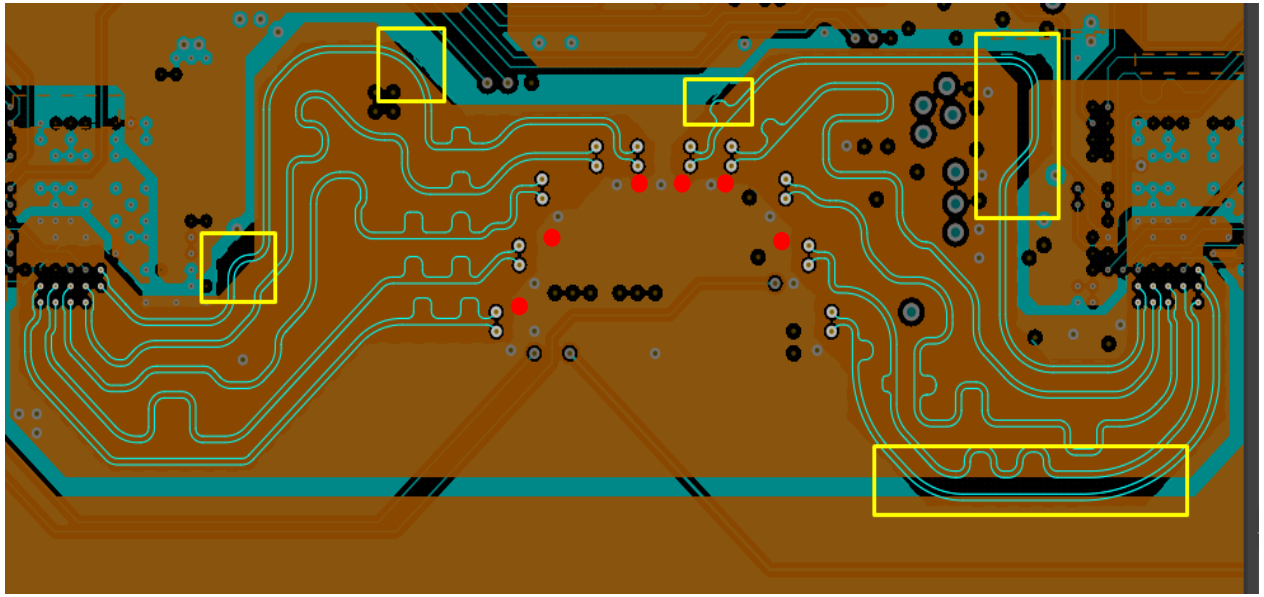
The PCB layout's performance can be increased by the following recommendations

MIPI Signals : FMCW Transceiver s to MCU

1. **Layer 3** traces has less spacing with GND polygon.
Need to increase spacing. It should be
5H (5 x 4= 20 mils)

2. **Layer 3** traces doesn't have the solid GND reference plane.

3. Add **GND** Vias near the Signal Layer Switching Vias.



Place Vias

Layout Recommendations

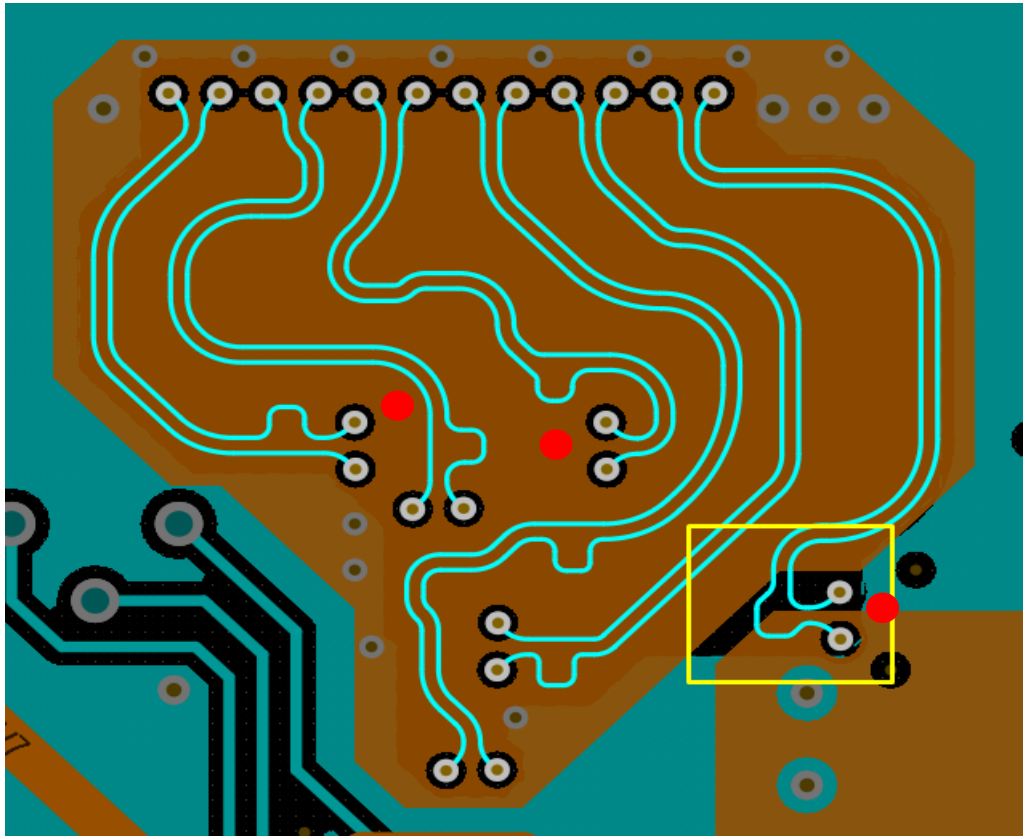
The PCB layout's performance can be increased by the following recommendations

LVDS Signals : MCU to Debug Connector

1. **Layer 3** traces has less spacing with GND polygon. Need to increase spacing/Clearance.

2. **Layer 3** traces doesn't have the solid GND reference plane. It has to be one reference plane without any splits.

3. Add **GND** Vias near the Signal Layer Switching Vias.



Place Vias

Layout Implementations

Suggested recommendations are incorporated to the PCB layout to enhance its performance.

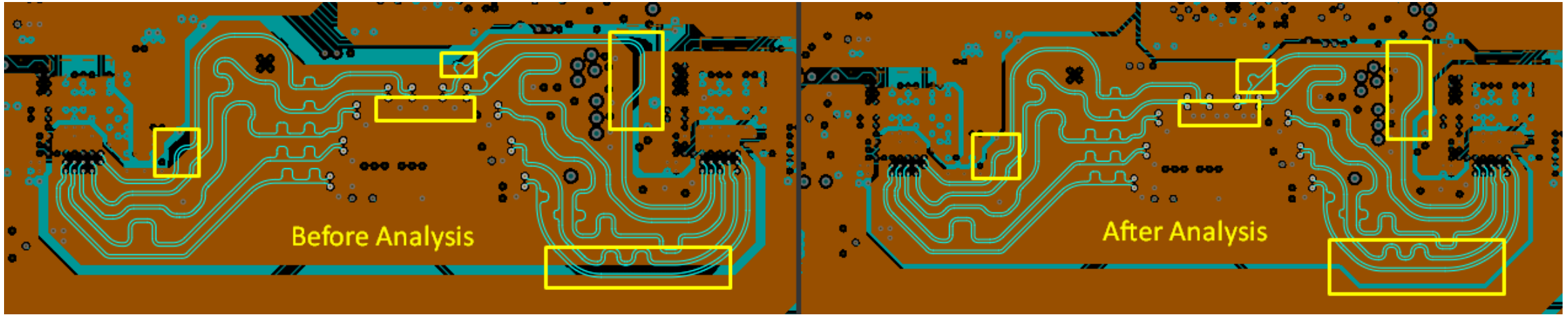
MIPI Signals : FMCW Transceiver s to MCU

Clearance:

Routing optimized to increase the spacing (5H - 20 mils) between GND and MIPI signal traces.

Vias:

Vias placed at the specified locations



Layout Implementations (Cont.)

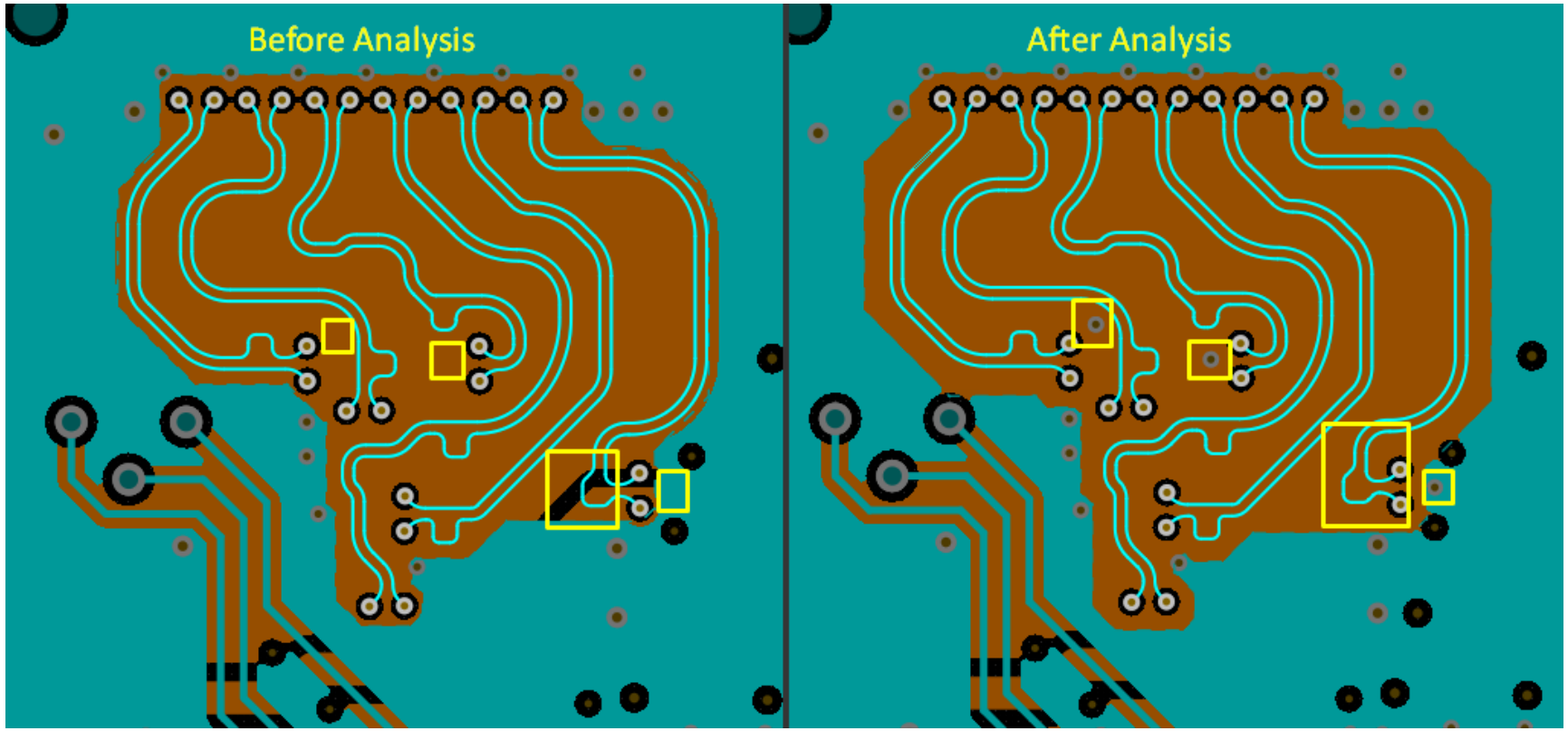
LVDS Signals : MCU to Debug Connector

Clearance:

Routing optimized to increase the spacing between GND and LVDS signal traces.

Vias:

Vias placed at the specified locations



Customer Testimonial

Excited to present a testimonial from a content client, emphasizing the success and positive impact of our Signal Integrity Analysis.

"Engaging the team for Signal Integrity (SI) Analysis was a game-changer for our project. Their meticulous approach ensured top-notch quality, uncovering potential issues and providing effective solutions. The detailed insights provided during the analysis were invaluable, contributing significantly to the overall success of our project. The cost-effective modifications to copper pours demonstrated their commitment to optimizing resources. Moreover, the timely delivery showcased their efficiency. We are highly satisfied with the quality, and timely delivery of the SI analysis, marking a significant enhancement in the reliability and efficiency of our electronic design!"

Conclusion

We delivered the client with a list of recommendations to make the HS signals work better and implemented changes in the layout design to boost overall performance. This demonstrated our unwavering commitment to delivering high-quality work and our technical expertise.

Our collaboration extends beyond technical aspects; it involves optimizing the signals in the layout for improved performance, by integrating our expertise with in-depth understanding of the client's specific requirements.

Our commitment is focused to delivering top-tier Analysis services, showcasing our unparalleled skills and unwavering reliability in achieving outstanding results.