





**Scope :** Stable and Reliable Power Distribution Network **Application :** ADAS - Automotive 4D Imaging Radar

In the automotive field, the Cascaded Radar Sensor Module finds application in various safety and driver-assistance systems. This module operates by emitting radar waves and analyzing their reflections to detect objects, obstacles, or vehicles in the vicinity.

The integration of a cascaded configuration elevates the sensor's capabilities, expanding its detection range with increased precision. This advanced technology, particularly in 4D imaging radar is vital for applications like adaptive cruise control, collision avoidance and other ADAS in automotives that contribute to boosting overall safety.



# **Power Integrity Analysis - Challenges**

The client asked to analyze the power integrity of the layout to meet out the required performance. Following are the list of challenges involved in the Power Integrity Analysis.

### **Challenges**

- ♦ Schematic optimization
- Placement of De-coupling capacitors
- Voltage Drop, Current Density & Via Current
- PDN Impedance
- Power Rail Ripple & Noise
- Ground bounce effects
- EMI effects
- ♦ Thermal Effect
- Internal Resistance of power planes
- Frequencies Outages







![](_page_3_Picture_0.jpeg)

![](_page_3_Picture_1.jpeg)

# **Study of Power Circuits**

The power circuits in the project is studied thoroughly to evaluate the performance of the power delivery network

L20 560nH XAL5020-561MEE

#### **Power Circuits**

- Buck Converter – 3.3V
- Boost Regulator -5V
- 1V8
- 1V2
- 1V0\_A
- 1V0\_B

=0.1uF

'P1 TP28

R58

1V7 

![](_page_3_Figure_12.jpeg)

![](_page_4_Picture_0.jpeg)

![](_page_4_Picture_1.jpeg)

### **Analysis Execution**

We executed the analysis in **HyperLynx** tool, to evaluate the power integrity performance of the layout.

Problems of power delivery network is identified from two perspectives: DC (IR Drop) and AC (Frequency)

Quantities to calculate include:

- ✓ Current Density
- ✓ Voltage Drop
- ✓ Via Current

![](_page_4_Picture_9.jpeg)

![](_page_4_Picture_10.jpeg)

![](_page_4_Picture_11.jpeg)

![](_page_4_Picture_12.jpeg)

![](_page_4_Figure_13.jpeg)

![](_page_4_Picture_14.jpeg)

![](_page_5_Figure_0.jpeg)

![](_page_6_Picture_0.jpeg)

![](_page_7_Picture_0.jpeg)

![](_page_8_Figure_0.jpeg)

![](_page_9_Picture_0.jpeg)

# **Layout Recommendations**

The PCB layout's performance can be increased by the following recommendations

- Net : 1V2
- 1. Increase the width of Cu pour at specified locations.
- 2. Add additional vias at the source point.
- 3. Add one via near Capacitor C4.

![](_page_9_Picture_7.jpeg)

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![](_page_10_Picture_0.jpeg)

### Layout Recommendations (Cont.)

#### Net : 1V2\_FILTERED

- 1. Increase the width of Cu pour at specified locations.
- 2. Increase the trace width to min. 20 mil on layer 5 under the U14 component.

![](_page_10_Picture_5.jpeg)

![](_page_10_Picture_6.jpeg)

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![](_page_11_Picture_0.jpeg)

![](_page_11_Picture_1.jpeg)

### Layout Recommendations (Cont.)

#### Nets : FE1\_VRF1\_FILTERED & FE2\_VRF2\_FILTERED

- 1. Increase the width of Cu pour at specified locations.
- 2. Increase the trace width in Bottom and Layer 5.
- 3. Add more vias to transfer power properly.

![](_page_11_Picture_7.jpeg)

![](_page_11_Picture_8.jpeg)

![](_page_12_Picture_0.jpeg)

![](_page_12_Picture_1.jpeg)

Suggested recommendations are incorporated to the PCB layout to enhance its performance.

Net : 1V2

- 1. Increased the width of Cu pour.
- 2. Vias added at source point and near capacitor C4.

![](_page_12_Picture_6.jpeg)

![](_page_12_Picture_7.jpeg)

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![](_page_13_Picture_0.jpeg)

![](_page_13_Picture_1.jpeg)

# Layout Implementations (Cont.)

#### Net : 1V2\_FILTERED

- 1. Increased the width of Cu pour.
- 2. Trace width increased to 20mil on Layer 5.

![](_page_13_Picture_6.jpeg)

![](_page_13_Picture_7.jpeg)

![](_page_13_Picture_8.jpeg)

![](_page_14_Picture_0.jpeg)

# Layout Implementations (Cont.)

#### Nets : FE1\_VRF1\_FILTERED & FE2\_VRF2\_FILTERED

- 1. Increased the width of Cu pour.
- 2. Trace width increased on Layer 5 & Bottom Layer.
- 3. Vias added for proper transfer of power.

![](_page_14_Picture_6.jpeg)

![](_page_14_Picture_7.jpeg)

![](_page_14_Picture_8.jpeg)

![](_page_14_Picture_9.jpeg)

![](_page_15_Picture_0.jpeg)

### **Customer Testimonial**

Excited to present a testimonial from a client, emphasizing the success and positive impact of our Power Integrity Analysis.

"We engaged the team for Power Integrity Analysis of PCB layout, and the results were exceptional. Their in-depth analysis uncovered potential issues that could have impacted the overall performance. The detailed insights provided, coupled with their practical recommendations along with cost-effective modifications to cu pours, allowed us to make informed decisions for optimizing our power distribution network. The team's expertise and commitment to delivering high-quality results were evident throughout the process. We are extremely satisfied with the quality, and timely delivery outcome of the analysis, and it has undoubtedly elevated the reliability and efficiency of our design!"

![](_page_15_Picture_4.jpeg)

Certified Compar

![](_page_16_Picture_0.jpeg)

![](_page_16_Picture_1.jpeg)

![](_page_16_Picture_2.jpeg)

We delivered the client with an optimized PDN layout design, incorporating layout enhancements to boost overall performance. This demonstrated our unwavering commitment to delivering high-quality work and our technical expertise.

Our collaboration extends beyond technical aspects; it involves optimizing the PDN in the layout for improved performance, by integrating our expertise with in-depth understanding of the client's specific requirements.

Our commitment is focused to delivering top-tier Analysis services, showcasing our unparalleled skills and unwavering reliability in achieving outstanding results.

![](_page_16_Picture_6.jpeg)