PCB Layout Design Optimization

[Battery Management System (BMS)]

Scope : Enhanced Performance and Cost Reduction

Application : Hybrid, Electric and Power Train Systems

A Battery Management System (BMS) is a critical component in rechargeable battery packs, ensuring optimal performance, safety, and longevity. It monitors individual cell conditions, balances charges, regulates temperature, and controls charging/discharging speeds.

In the realm of electric vehicles, BMS plays a pivotal role, especially in Advanced Driver Assistance Systems (ADAS), contributing significantly to the efficiency and reliability of battery systems in the automotive industry.

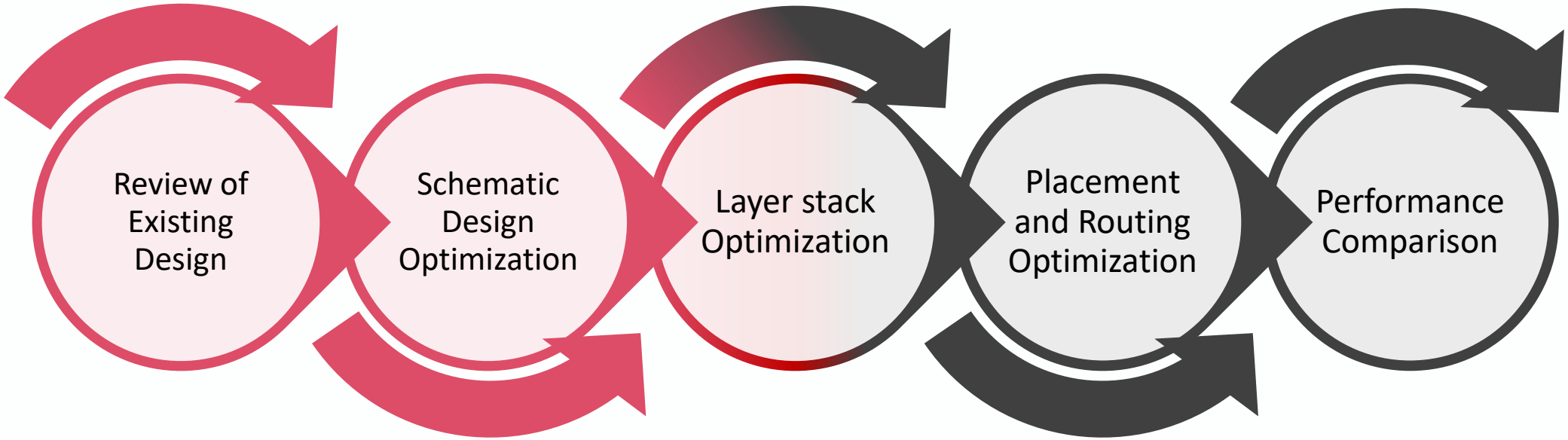
Layout Optimization - Challenges

The client encountered a challenge with the functionality of the existing circuit design. Specifically, in BMS module. Requires design optimization to improve the performance and optimize the layout for cost reduction.

Challenges

- Schematic optimization
- Usage of Existing PCB raw Materials
- Insulation design margin
- Layer Stack-up
- Space constraints
- Components Placement
- Density of the Layout
- Manufacturability
- Cost considerations
- No heavy redesign to the Existing Design.
- Comparing performance with the existing design

Layout Design Optimization - SoW



Existing Design of BMS

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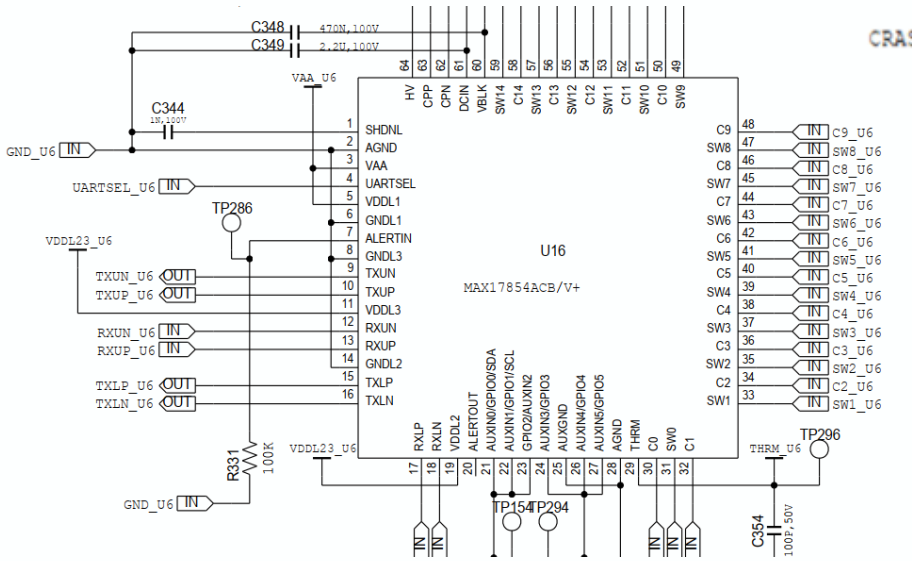
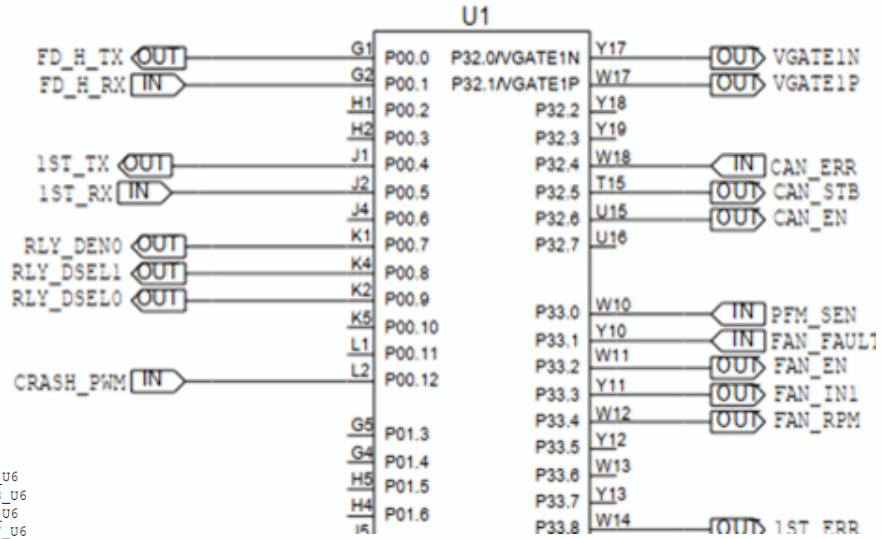
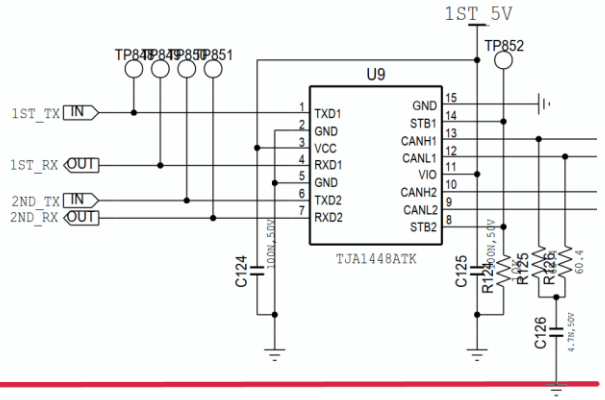
The existing layout incorporates Maxim's MAX17854ACB/V+ circuits to monitor 64S battery packs, encompassing both the High Voltage (HV) and Low Voltage (LV) sides on the PCB layout.

Main Circuits

- BMS Monitor IC circuits (64S Battery Pack)
- MCU & SBC circuits
- CAN Communication circuits
- Protection / Monitor circuits
- Relay Circuits







Existing Layout Design

The existing layout encompassing both the High Voltage (HV) and Low Voltage (LV) sides to monitor 64S battery packs.

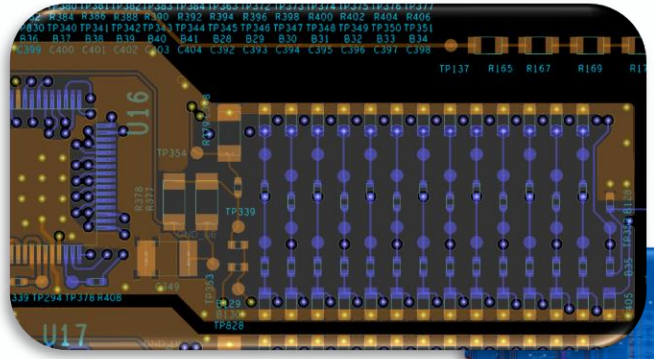
PCB Constraints

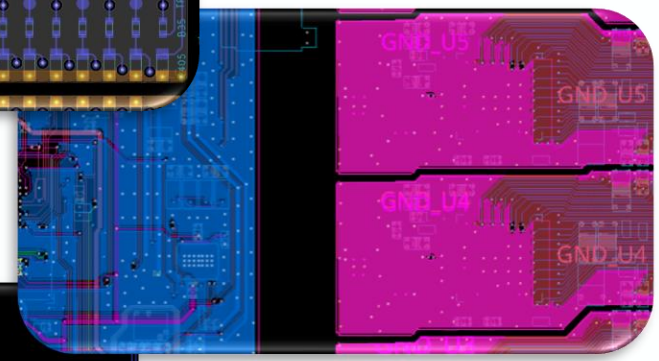
- Total Components – 3357
- Layer Count – 6 Layers
- Total Connections - 4473
- PCB Dimensions – 218 x 138mm
- BMIC Circuits – 6 BMIC
- UART & CAN Communication
- Unique GND for each BMIC section

Layer structure

Layer	Drill	Material Composition
		Solder Resist
		Cu Plating (Cap plating)
		Cu Plating
1	TOP	C/F 1/3 Oz
		Pre-Preg 2116
2		Copper 1 Oz
		T/C 0.50 T
3		Copper 1 Oz
		Pre-Preg 7628
4		Copper 1 Oz
		T/C 0.50 T
5		Copper 1 Oz
		Pre-Preg 2116
6	BOT	C/F 1/3 Oz
		Cu Plating
		Cu Plating (Cap plating)
		Solder Resist

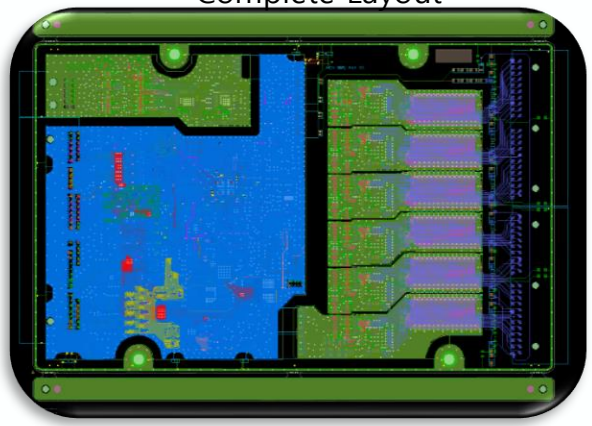
1(TOP), 2(GND Plane) Layer

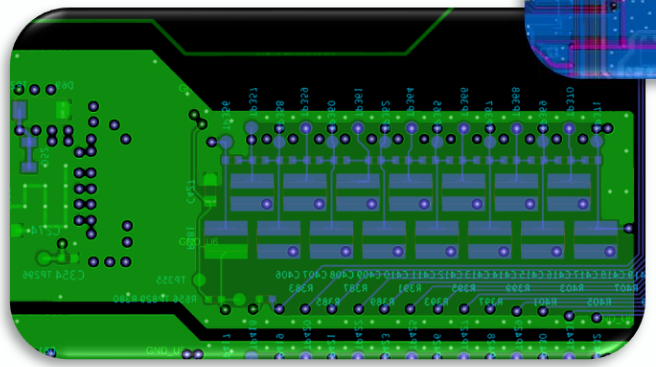




3(Pattern), 4(Pattern, GND Plane)

Complete Layout





5(GND Plane), 6(BOT) Layer

Layout Design Optimization – Execution

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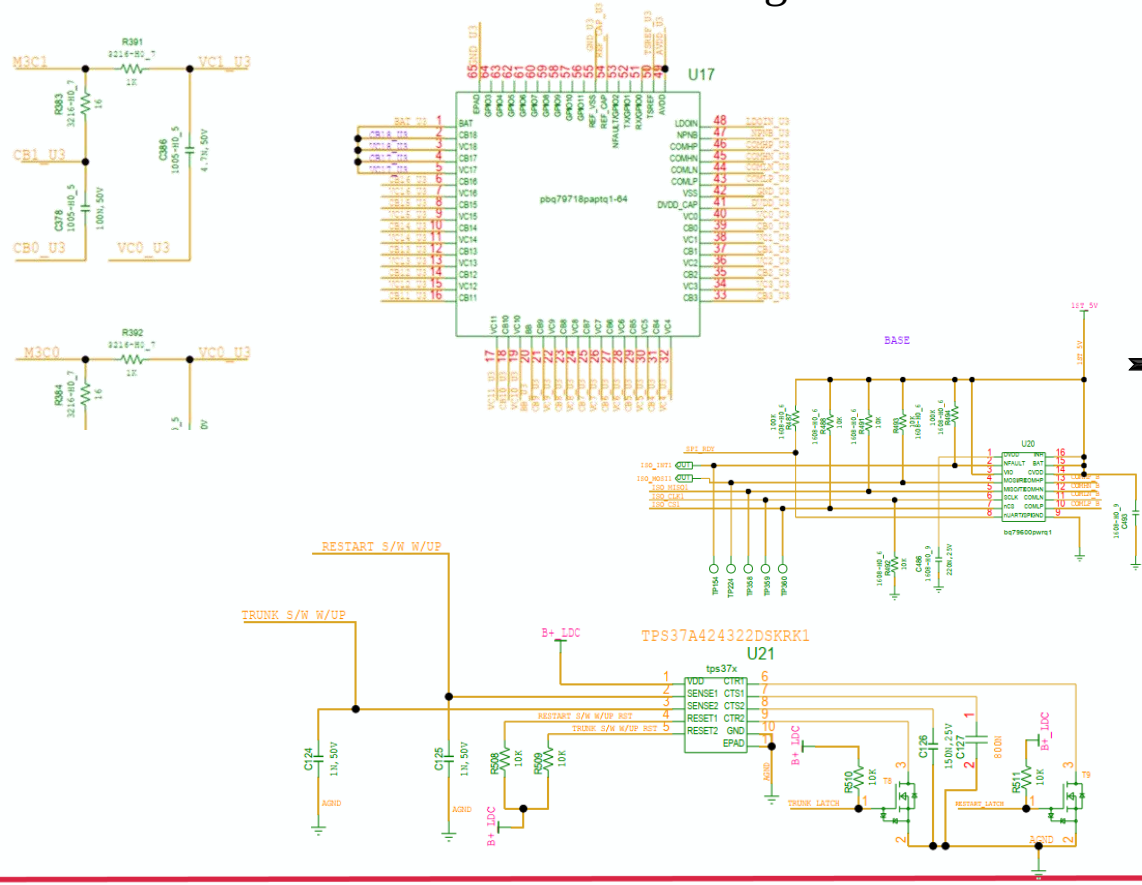
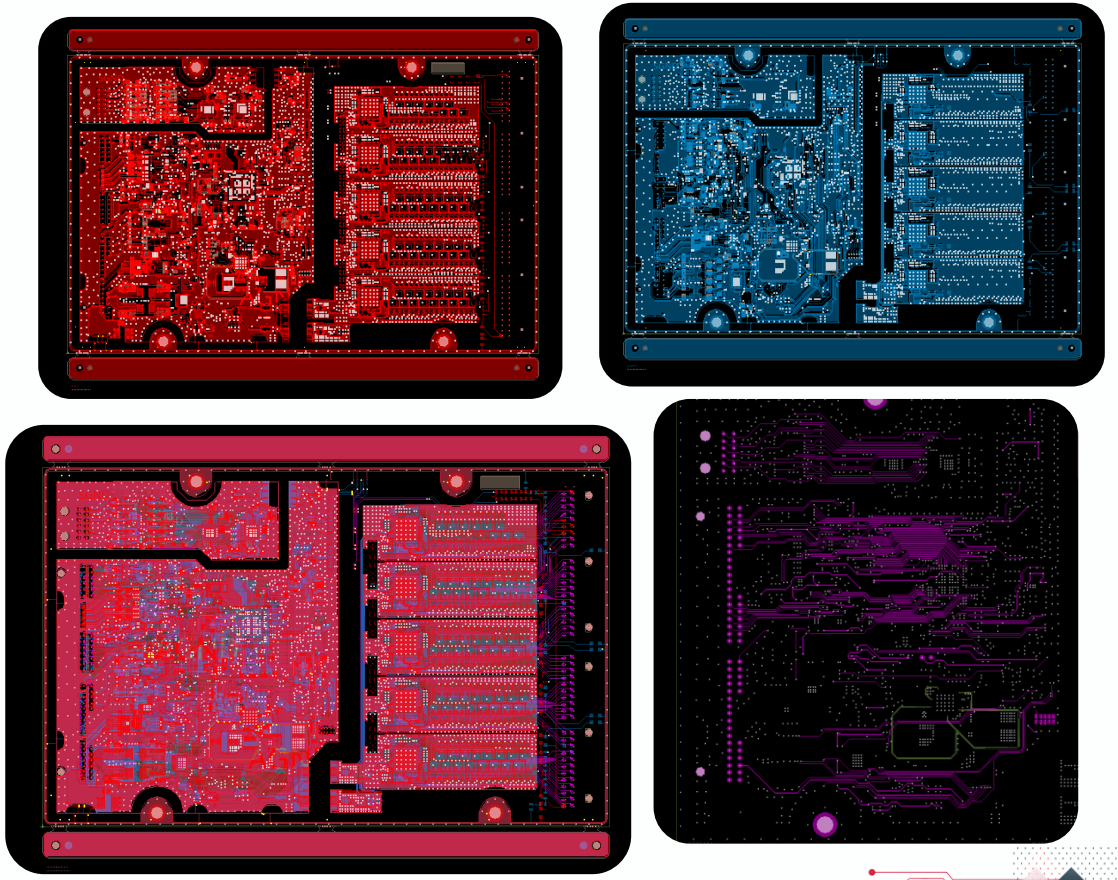
Schematic Optimization:

To enhance the design's performance, a new schematic design with alternative components was proposed to reduce the BOM cost. Furthermore, the PCB layer count was minimized, contributing to an overall reduction in design costs.



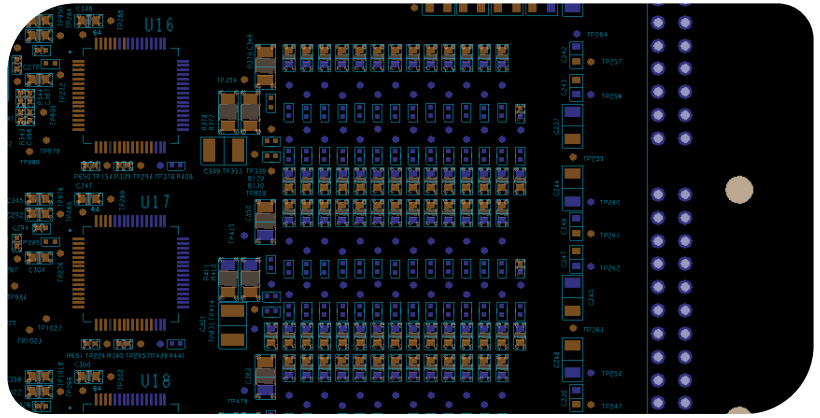


Layout Design Optimization – Execution(Cont.)

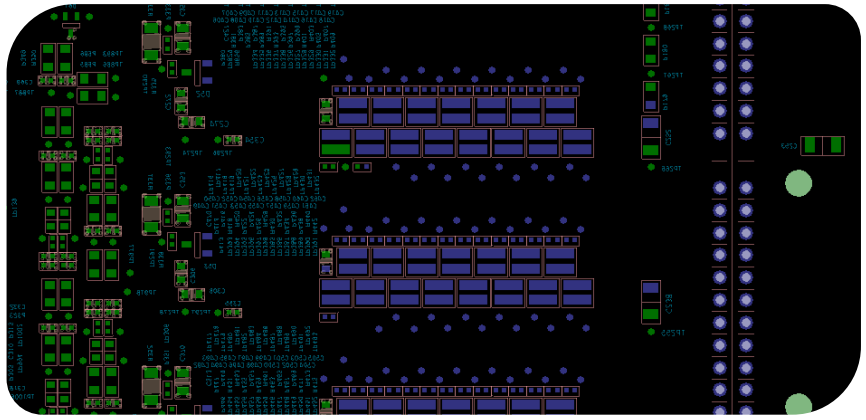
The PCB layout is optimized step by step, ensuring improved performance and cost-effectiveness.

Placement: New optimized schematic design (with reduced components) led to optimized placement of components

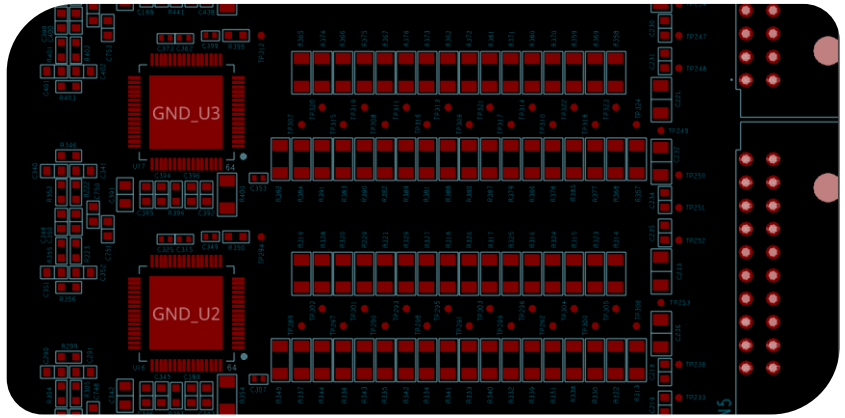
Existing Layout:



Top
(LV Side)



Optimized Layout:

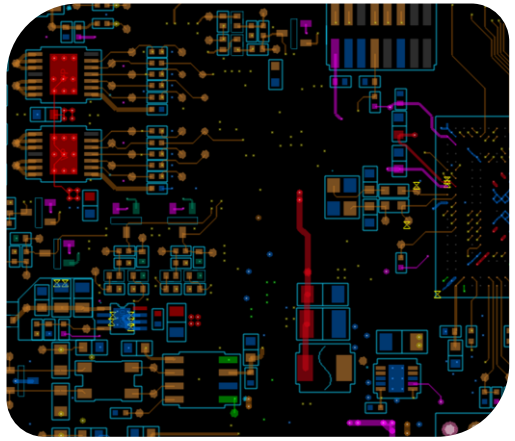


Bottom
(LV Side)

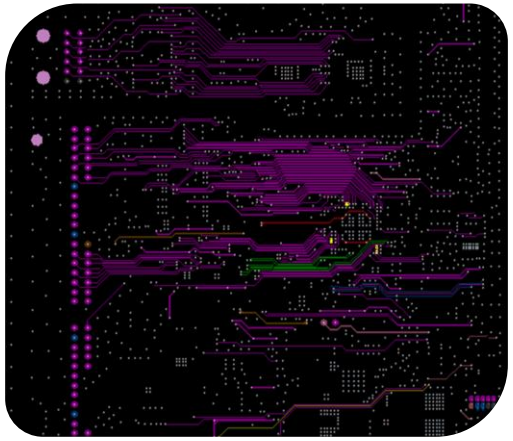
Layout Design Optimization – Execution(Cont.)

Routing: Existing L3 and L4 routings are optimized in Top, L3 and Bottom Layers due to reduced layer stack-up.

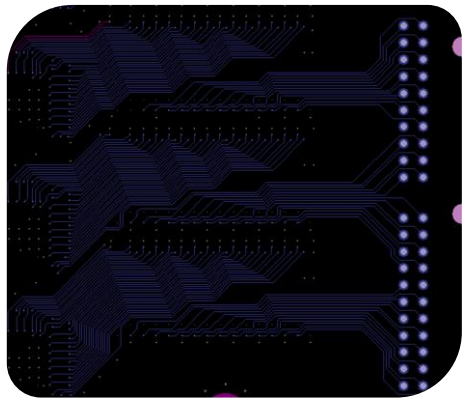
Existing Layout:



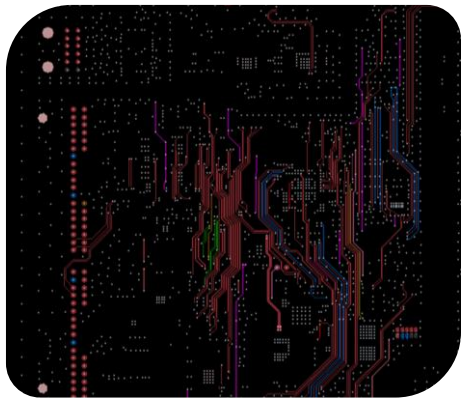
TOP



L3 – HV side

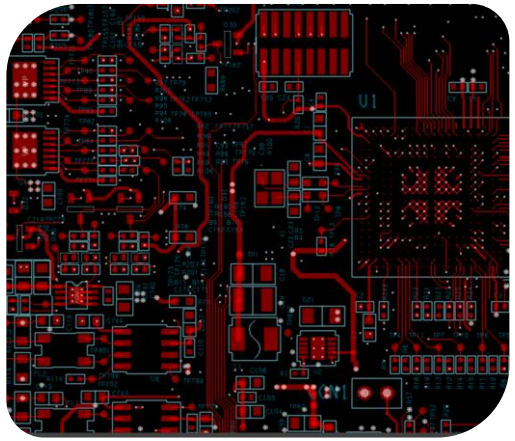


L3 – LV side

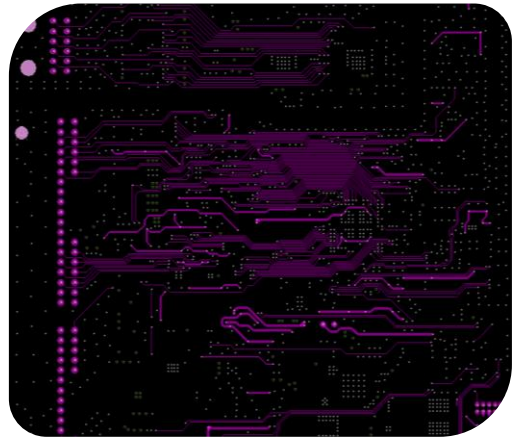


L4

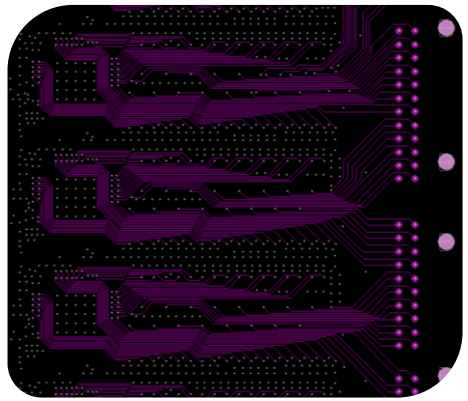
Optimized Layout:



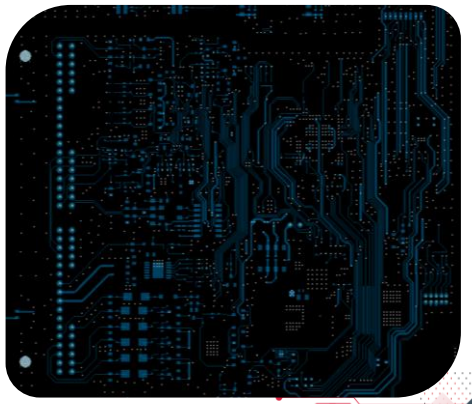
TOP



L3 – HV side



L3 – LV side

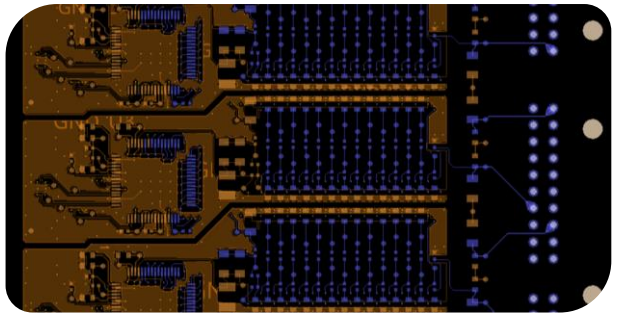


BOTTOM

Layout Design Optimization – Execution(Cont.)

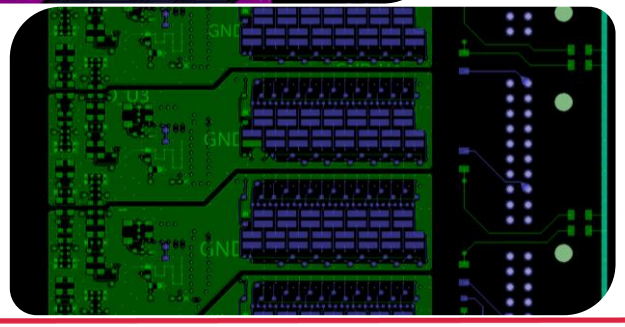
Cu Pours: Pours are optimized to ensure uniformity and provided sufficient thermal management through numerous vias and required isolation between each stack.

Existing Layout Design:



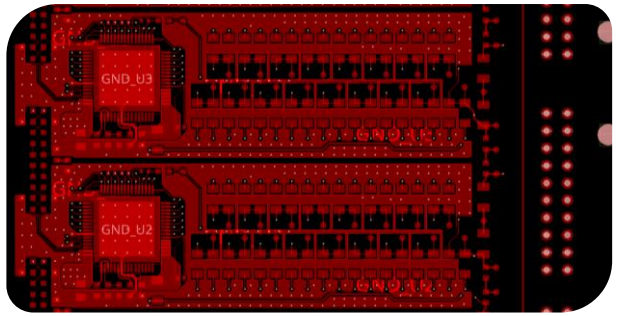
Top
(LV Side)

L3
(LV Side)

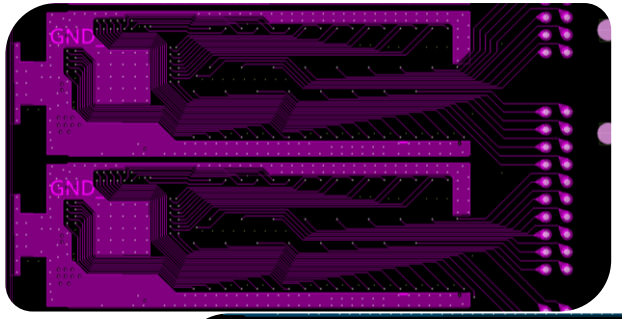


Bottom
(LV Side)

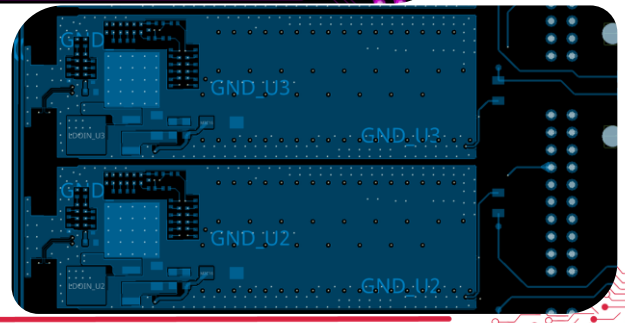
Optimized Layout Design:



Top
(LV Side)



L3
(LV Side)



Bottom
(LV Side)

Layout Design Optimization – Execution(Cont.)

Usage of Existing Insulating Materials: CTI Test

When creating a 4-layer PCB, it's essential to assess the insulation design margin in the layer section, taking into account the CTI grade specified by the material manufacturer for the PCB.

Requirement: Material needs to endure the Maximum withstand voltage between adjacent floors (320V)

Existing Layout Design:

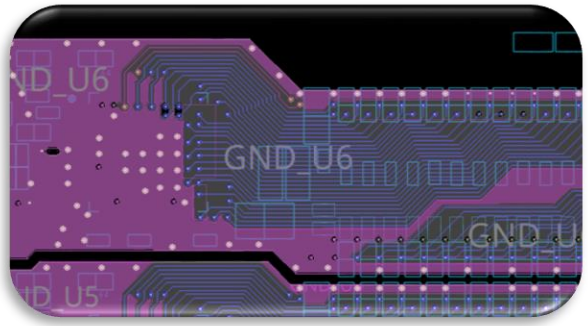
Used Doosan DS-7402LC / DS-7402 CTI 4th grade 175V

175V * 2 = 350V (more than 320V) design through GND plane insertion, applying insulation for the maximum withstand voltage.

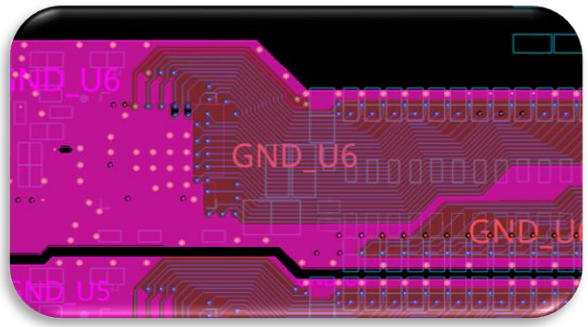
Doosan DS-7402LC / DS-7402

Dielectric breakdown	>30	kV/mm	AC	IPC-TM-650 2.5.6.2A
Comparative tracking index	4	-	As received	IEC 60112
Water Absorption	0.11	%	D-24h/23°C	IPC-TM 2.6.2.1A

2(GND Plane), 3(Pattern) Layer



3(Pattern), 4(GND Plane) Layer



Range – Tracking index (volts)	Assigned PLC
600 ≤ TI	0
400 ≤ TI < 600	1
250 ≤ TI < 400	2
175 ≤ TI < 250	3
100 ≤ TI < 175	4
0 ≤ TI < 100	5

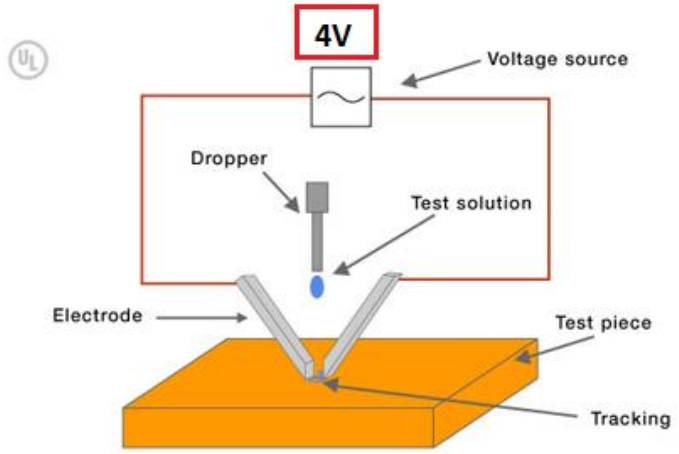
Layout Design Optimization – Execution(Cont.)

Usage of Existing Insulating Materials: CTI Test

Optimized Layout Design:

The maximum withstand voltage between adjacent floors in the optimized design will be **4V** as per basic understanding (Distributed lines). While considering for a stack as lumped (16 patterns together) **64V** is the maximum withstand voltage.

There is sufficient insulation margin for the maximum withstand voltage (175V) while using the same PCB raw material (Doosan DS-7402LC / DS-7402 CTI 4th grade 175V) as Existing design.



Layout Design Optimization – Result

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Optimized Layout Design: PCB Layout optimized to 4L design from 6L design without change in the dimensions of the PCB.

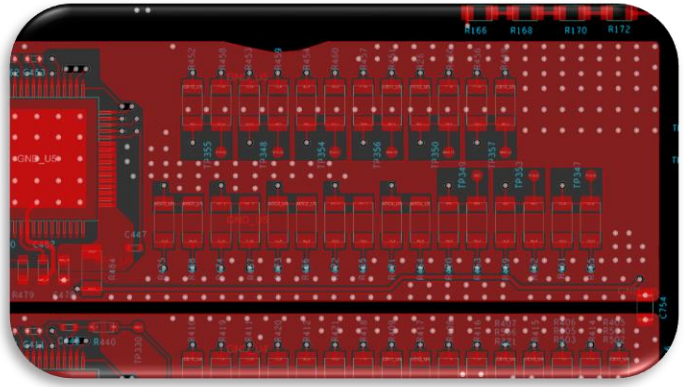
PCB Constraints

- Total Components – 2321
- Layer Count – 4 Layers
- Total Connections - 3398
- PCB Dimensions – 218 x 138mm
- BMIC Circuits – 5 BMIC
- Unique GND for each BMIC section

4LAYER 표준 lay-up. 1oz

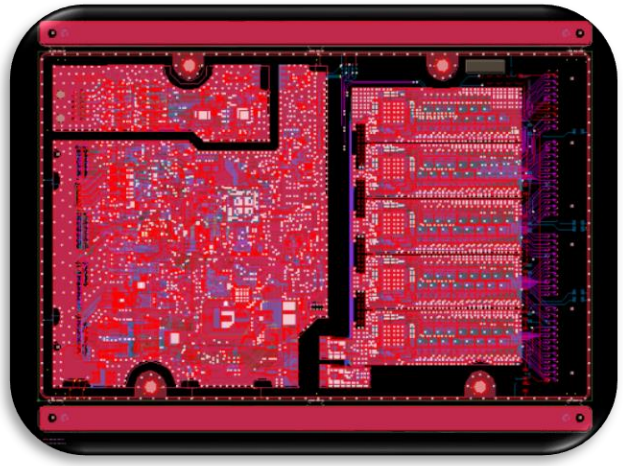
최종두께 : 1.6T(PP 7628 0.18t)

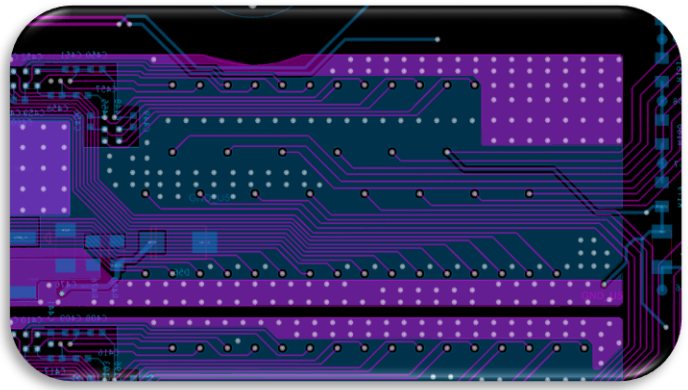
LAYER		MATERIAL	T(mm)	
PSR			0.0150	
1		Plating(도금)	0.0550	1.COMP
		1 oz		
PP		Prepreg 7628	0.1800	
2	T/C 1.1T 1/1	1 oz	0.0300	2.INT
		Core 1.04T	1.0400	
3		1 oz	0.0300	3.INT
PP		Prepreg 7628	0.1800	
4		1 oz	0.0550	4.SOLD
		Plating(도금)		
PSR			0.0150	
THICKNESS			1.600	



1(TOP), 2(GND Plane) Layer

Optimized Design – 4 Layer





3(Pattern), 4(BOT) Layer

Layout Design Optimization – Outcome

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In the new optimized layout design, enhanced the performance of the Layout, and achieved remarkable **20%** (min.) reduction of the overall design cost.

1. BMIC changed to TI chip in BMS with added cell monitoring.
2. PCB Design from 6 Layer to 4 Layer.
3. Existing PCB raw Materials are used
4. Insulation design margin achieved same as existing design
5. Optimized Components Placement
6. Density of the board reduced
7. Provided required thermal management
8. Improved performance

GigHz
A Global Engineering partner

An ISO-27001 ISMS Certified Company

Customer Testimonial

Delighted to share a testimonial from a satisfied client, underscoring the success and positive influence of our PCB Layout Design Optimization.

"We entrusted the team with the challenging task of optimizing our PCB layout, and the results were beyond impressive. Their innovative solutions and meticulous attention to detail not only improved the overall performance but also led to significant cost savings. The team's commitment to delivering high-quality work within a tight timeframe demonstrated their expertise and reliability. We are extremely satisfied with the outcome of the PCB layout optimization, and it has undoubtedly elevated the efficiency of our design. We look forward to continued collaboration with this talented and reliable team!"

Conclusion

We presented the client with an optimized layout design that outperforms the existing one, incorporating enhancements in both schematics and layout to boost overall performance. This underscores our unwavering commitment to delivering high-quality work and highlights our technical expertise.

Our collaboration extends beyond technical aspects; it encompasses optimizing the layout design for improved performance, achieved by seamlessly integrating our expertise with in-depth understanding of the client's specific requirements.

We are committed to delivering top-tier ECAD services, showcasing our unparalleled skills and unwavering reliability in achieving outstanding results.