Design & Signal Integrity Analysis of Mirror ISP Layout

Scope : Design & Signal Integrity analysis

Application : ADAS with Enhanced Performance

Designing a PCB layout encompasses creating layout that aligns with the specified requirements. Signal integrity practices into PCB layout and routing is to ensure that a signal is not degraded as it transfers from a driver component to a receiver.

This signifies the signal's ability to propagate without distortion. It gives the measurement of the amount of signal degradation when the signal travels from the driver to receiver. The outcome of analysis leads to improvise the performance of the layout and application in the field of Autonomous Driver Assistance Systems (ADAS).

Design & Signal Integrity Analysis

Challenges

- Fine Pitch BGA- 0.65mm
- Blind Buried Vias
- High Speed signals – MIPI, LVDS
- Length Matching
- Signal Quality
- CLK & Data topology
- Propagation Delay
- Cross Talk noise
- EMI/EMC & GND bounce

Requirements

- Fine-Tune Component Placement
- Keep things separate – Power & HS Signals
- Ensure propagation without distortion.
- Proper type of transmission lines
- Controlled Impedance
- Eliminate Overshoot and undershoot in digital signals.
- Avoid data corruption
- Reliable and optimal performance

Layout Design & SI Analysis - SoW

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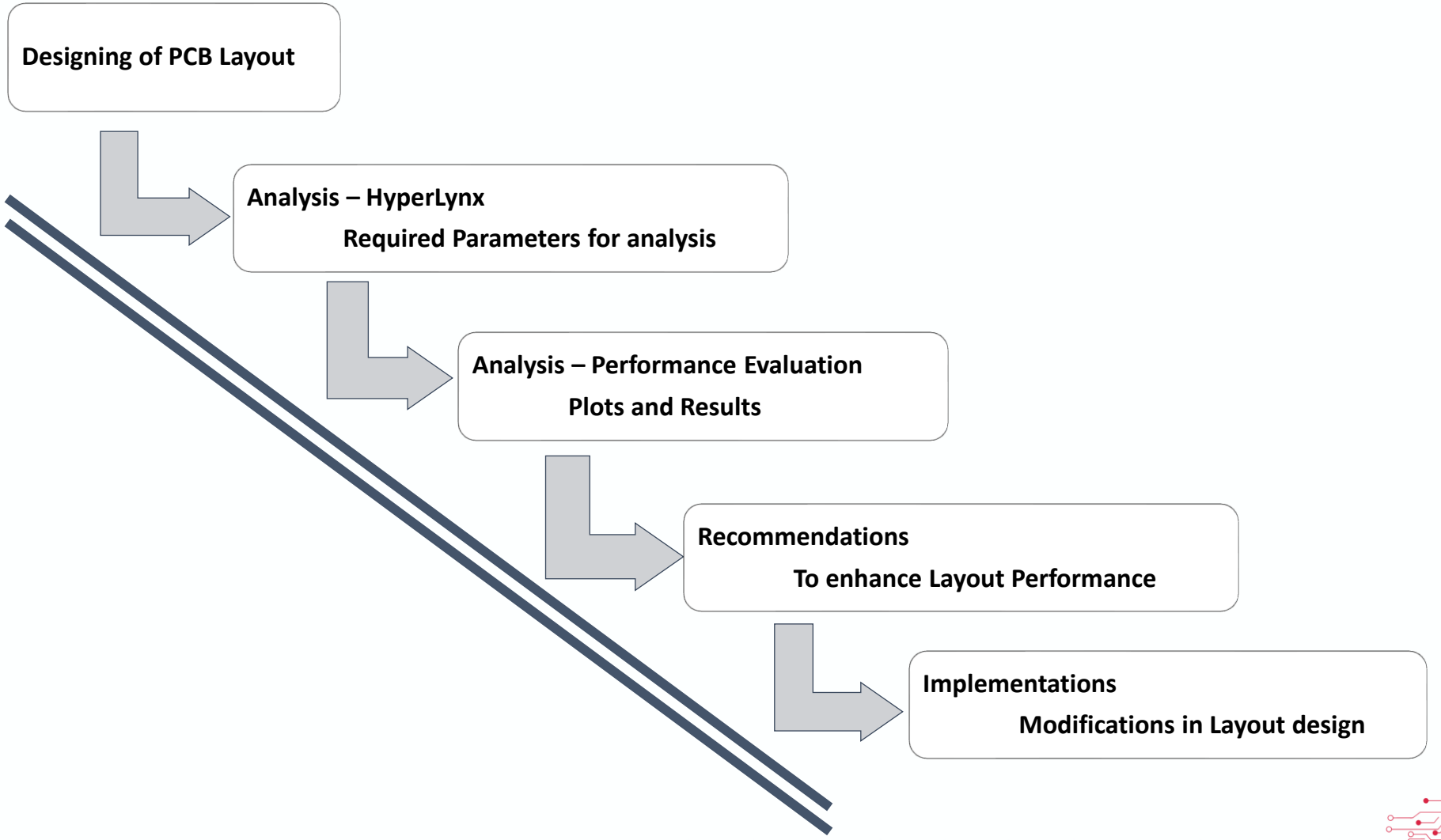


Design of PCB Layout – How we executed?

This layout includes circuits like De-Serializer, Image Signal Processor, and Display Controller. They work together for the TFT Display, showing the signals from the camera in an Autonomous application. The Layout design is completed based on the instructions and requirements from the client.

Power Circuits

- +12V
- SEPIC Power – 9.5V
- Coax Power – 8.6V
- +3.3V
- +5V
- +2.0V
- +1.8V
- +1.5V
- +0.9V

Sensor Circuit

- Ambient Light Sensor
- Toggle sensor

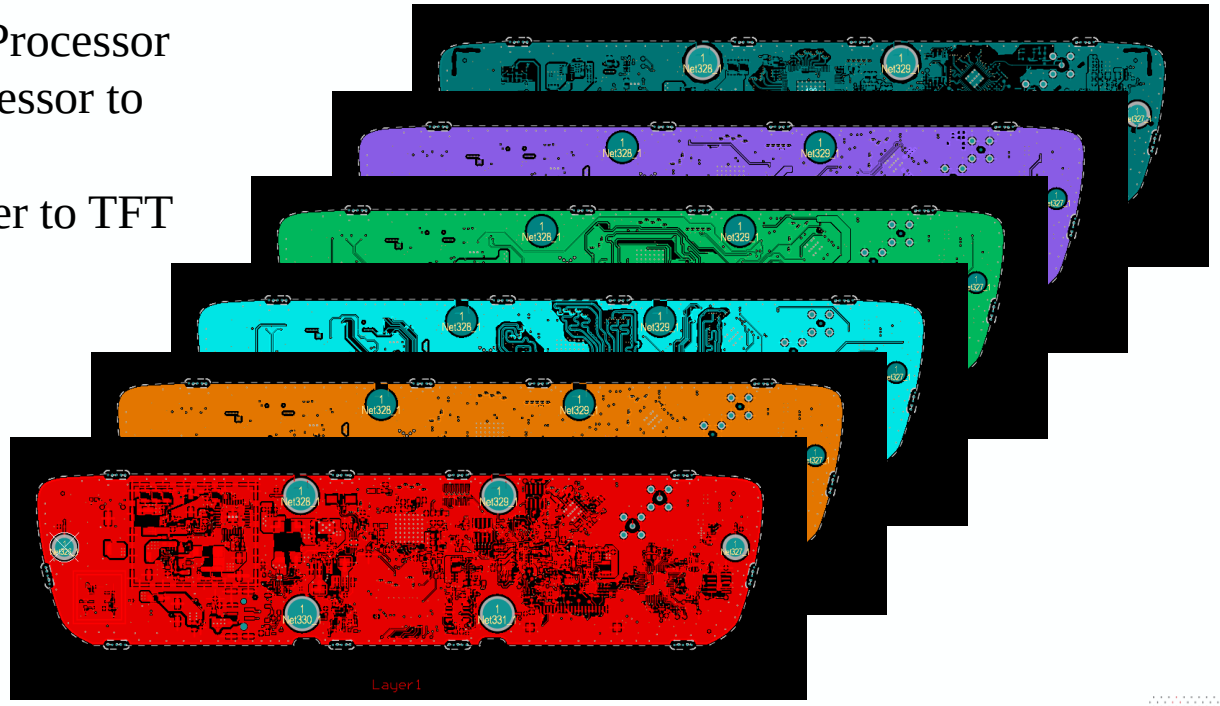
High Speed Signals

- MIPI – De-ser to Video Processor
- MIPI_OUT - Video Processor to Display controller
- LVDS - Display controller to TFT Display connector

High Speed Signal Circuit

- De-serializer
- Image Signal Processor
- Display Controller

Finished Layout



*The finished layout design file needs to be analyzed to assess its performance.

Analysis – How we executed?

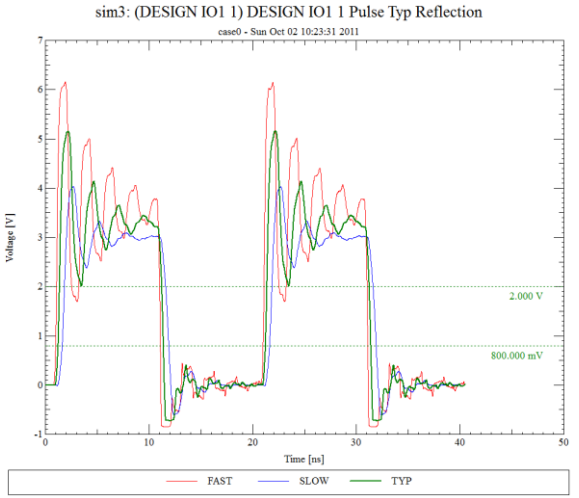
We executed the analysis in **HyperLynx** tool, to evaluate the signal integrity of the layout.

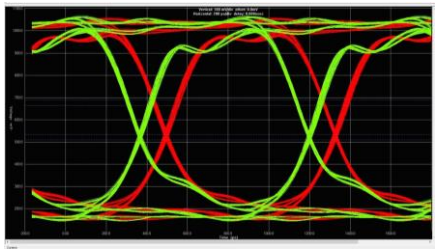
Signal integrity analysis aims to identify operation problems in two levels: Interconnect level and Systems-level.

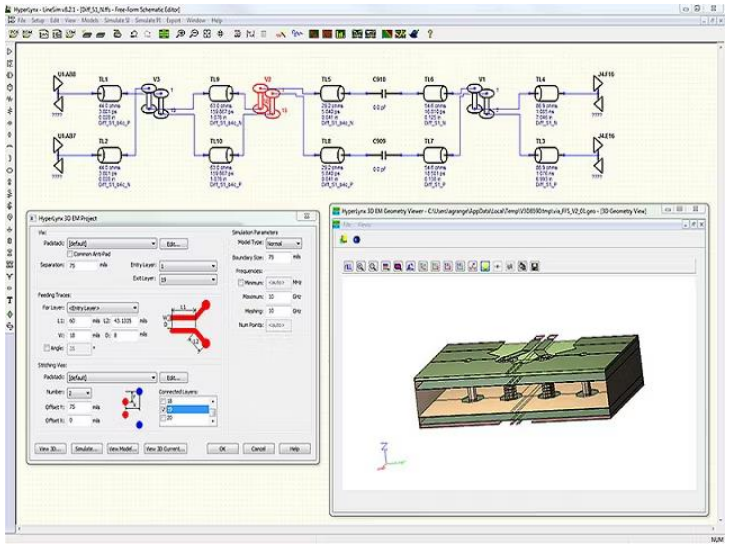
Interconnects comprise pads, transmission lines, vias between PCB layers, and any components encountered along the way.

At the systems level, there are driver and receiver components that generate and interpret the signal, respectively.

- ✓ Interactions between the PDN and high-speed signals.
- ✓ Result of Simultaneous Switching Noise (SSN).
- ✓ Return path discontinuities.



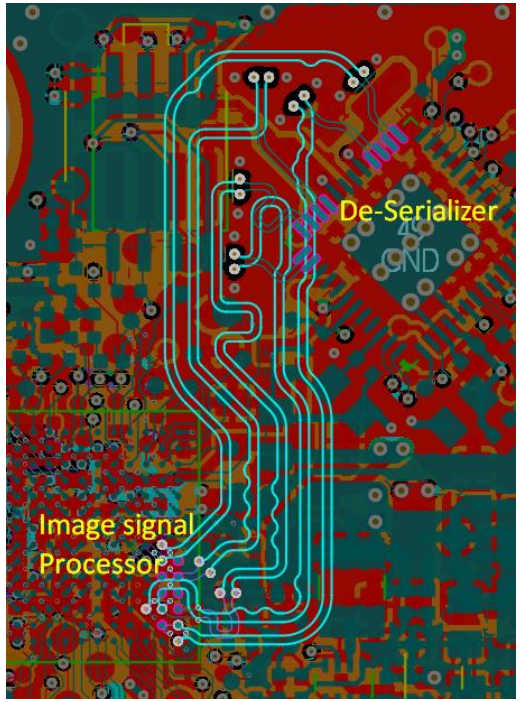




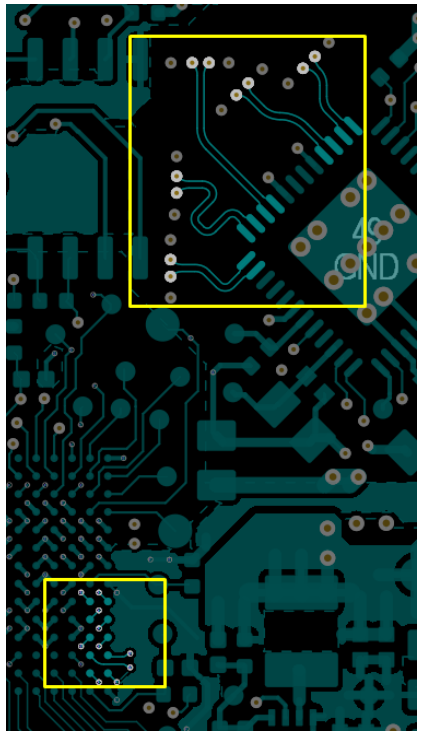
Analysis – How we executed?

MIPI signals – De-serializer to Image signal Processor.

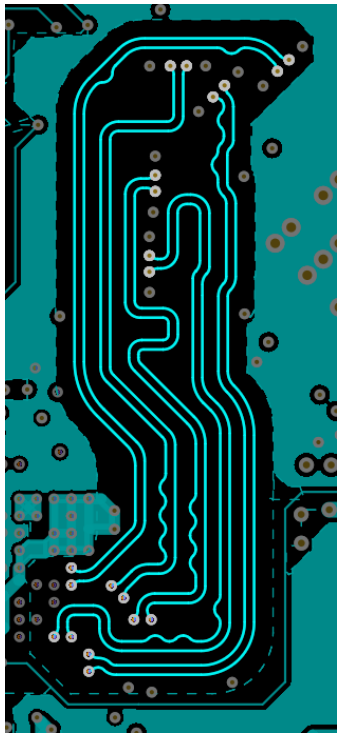
Layout - Routing



Layer 6 (Bottom)



Layer 3



Trace Lengths

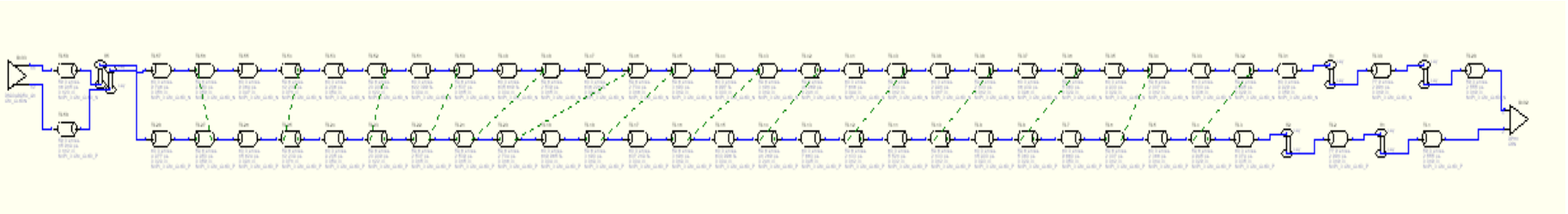
10 Nets (0 Highlighted)

Name	Node ...	Signal ...	Total P...	Routed ...	Unr...
MIPI_3.CSI_CLK0_N (-)	2	1402.428	0	1403.295	0
MIPI_3.CSI_CLK0_P (+)	2	1402.587	0	1403.415	0
MIPI_3.CSI_D0_N (-)	2	1400.092	0	1401.268	0
MIPI_3.CSI_D0_P (+)	2	1400.145	0	1401.489	0
MIPI_3.CSI_D1_N (-)	2	1400.186	0	1401.097	0
MIPI_3.CSI_D1_P (+)	2	1400.46	0	1401.25	0
MIPI_3.CSI_D2_N (-)	2	1400.088	0	1400.167	0
MIPI_3.CSI_D2_P (+)	2	1400.943	0	1401.289	0
MIPI_3.CSI_D3_N (-)	2	1400.092	0	1401.043	0
MIPI_3.CSI_D3_P (+)	2	1400.448	0	1401.289	0

CLK and Data's are routed with same trace length (closely)

Analysis – Plots and Results (Cont.)

Topology - CSI - CLK



Analysis Parameters – Requirements

As per video processor

VinH = 300mV

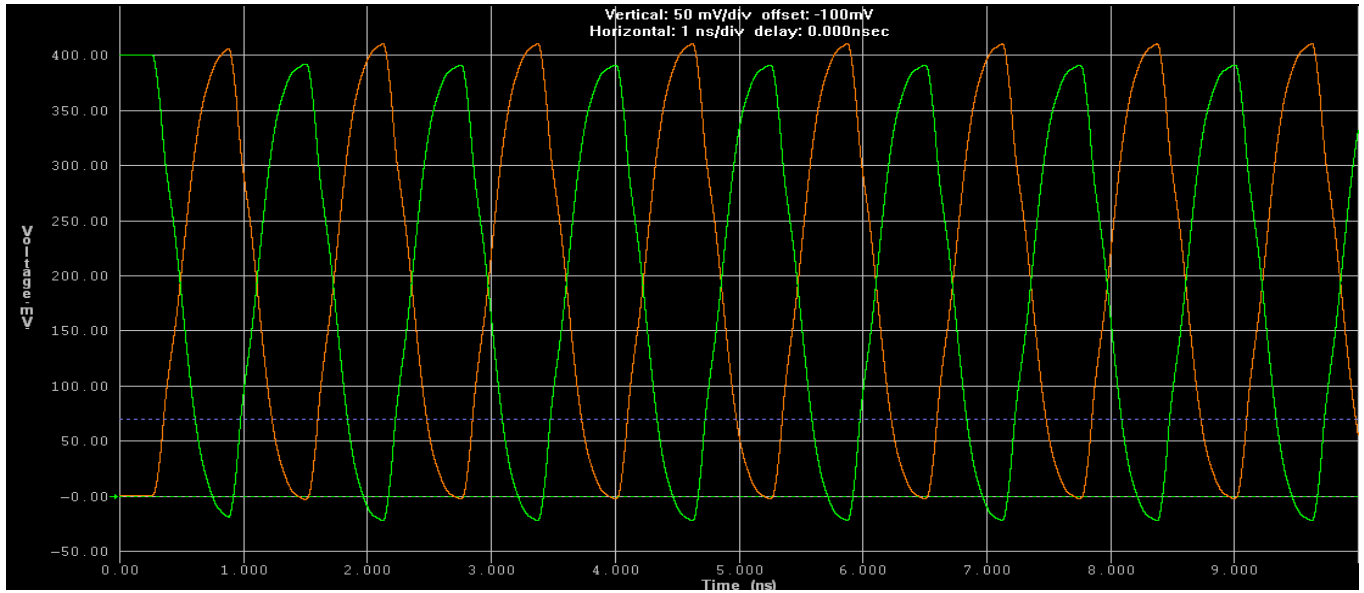
VinL = 100mV

MIPI CSI interface standard requirements

VinH = 235mV

VinL = 165mV

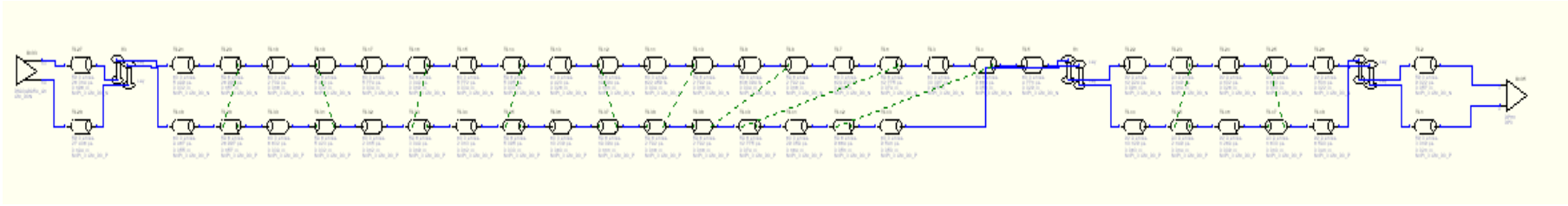
Analysis Result



Both the values are meeting the requirement and the results are passing

Analysis – Plots and Results (Cont.)

Topology - CSI - DATA



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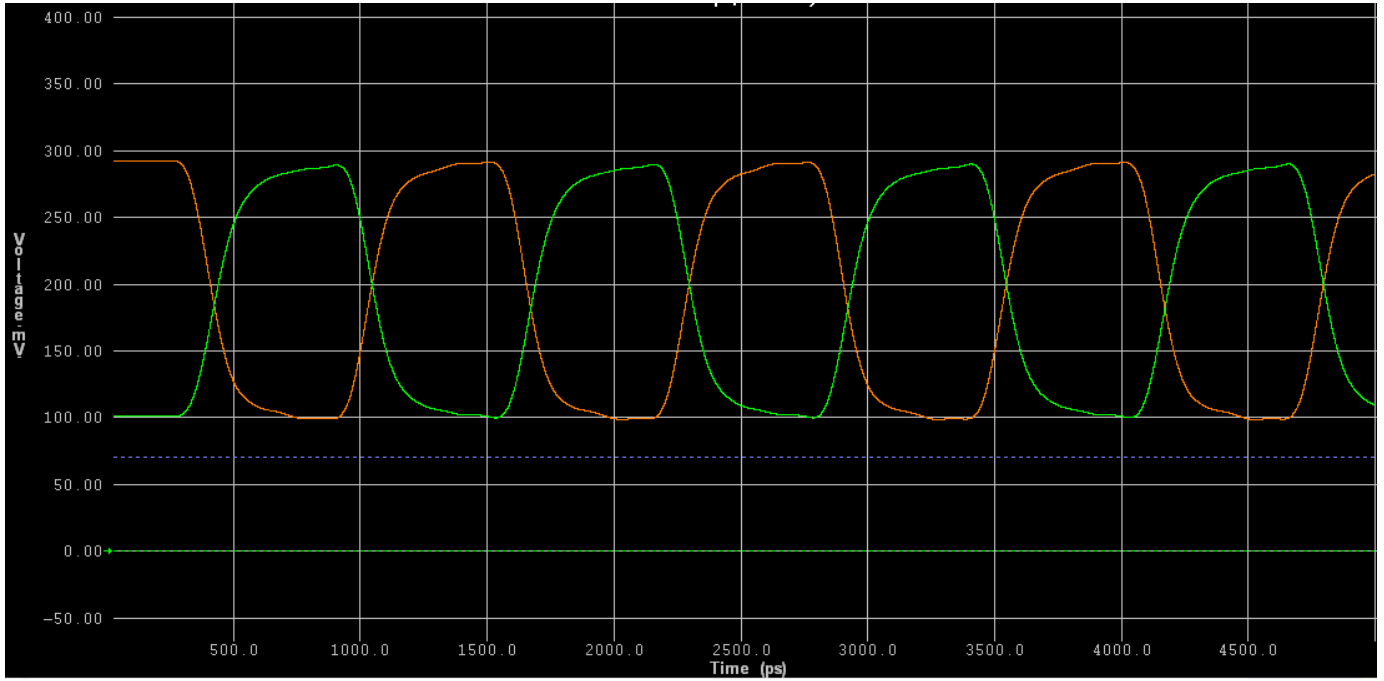
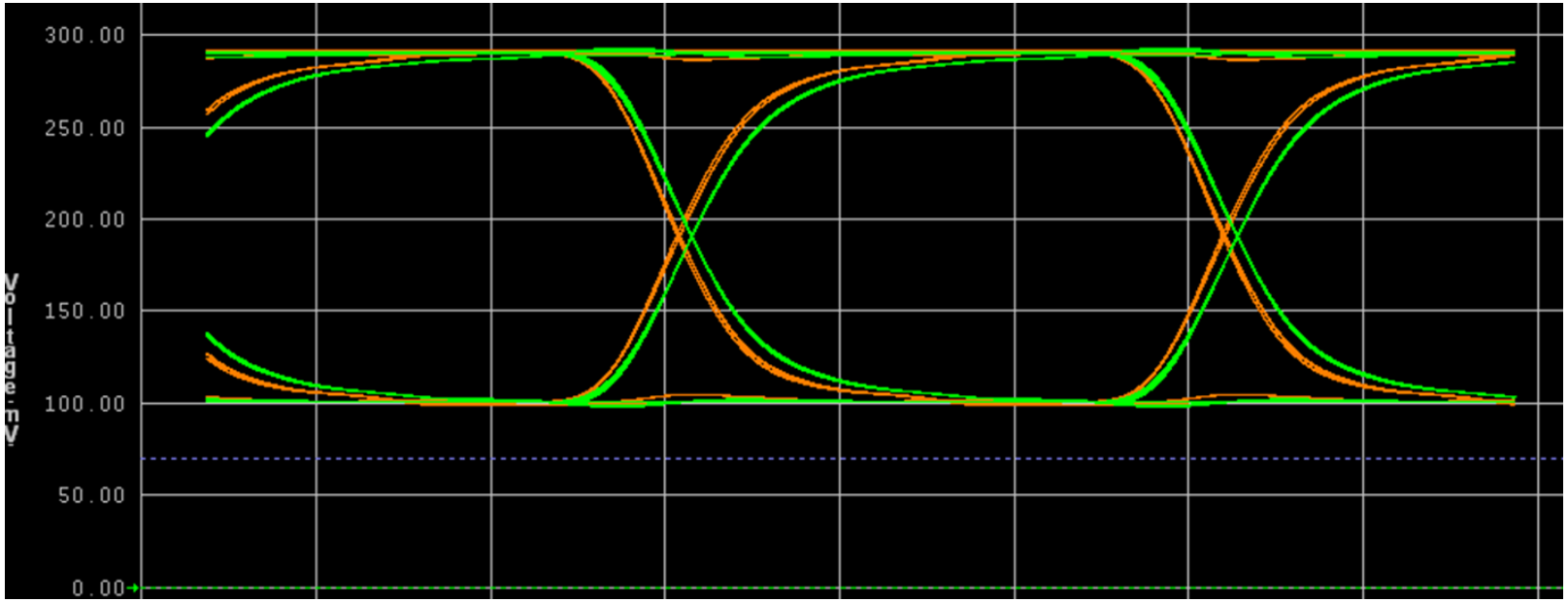


Analysis – Plots and Results (Cont.)

Analysis Result

Topology - CSI - DATA

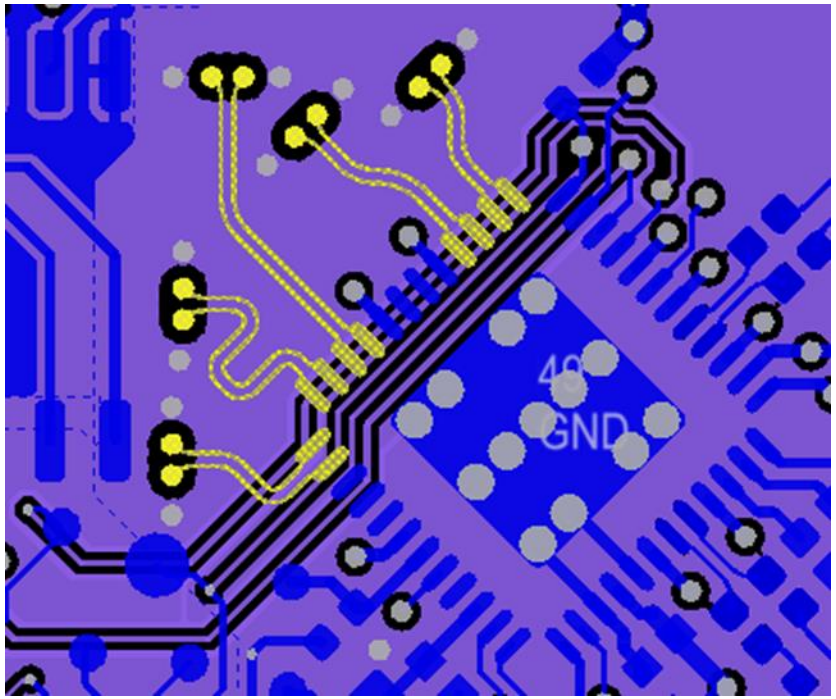


As per MIPI CSI interface actual requirements is VinL =165mv and VinH=235mv, which is **meeting the requirement and the results are pass.**

As per video processor (GW5410) requirements, the VinL =100mv and VinH=300mv, Which is **not possible to meet the requirements** due to DS90UB954 driver strength. Please check with chip vendor about the VinL & VinH values, if they are ok with standard values.

Layout Recommendations (Cont.)

Layer 6 traces and pads doesn't have the solid GND reference plane.



De- Serializer

Layer 5 traces doesn't have the solid GND reference plane.

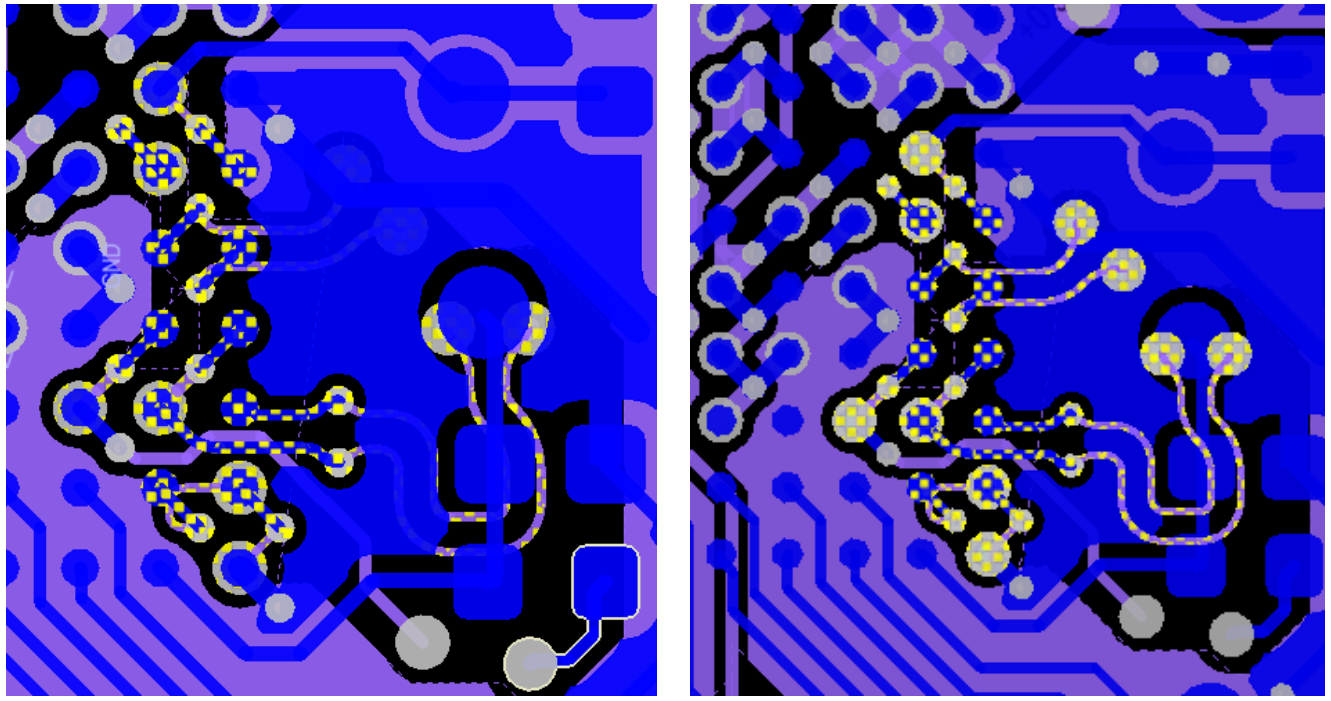
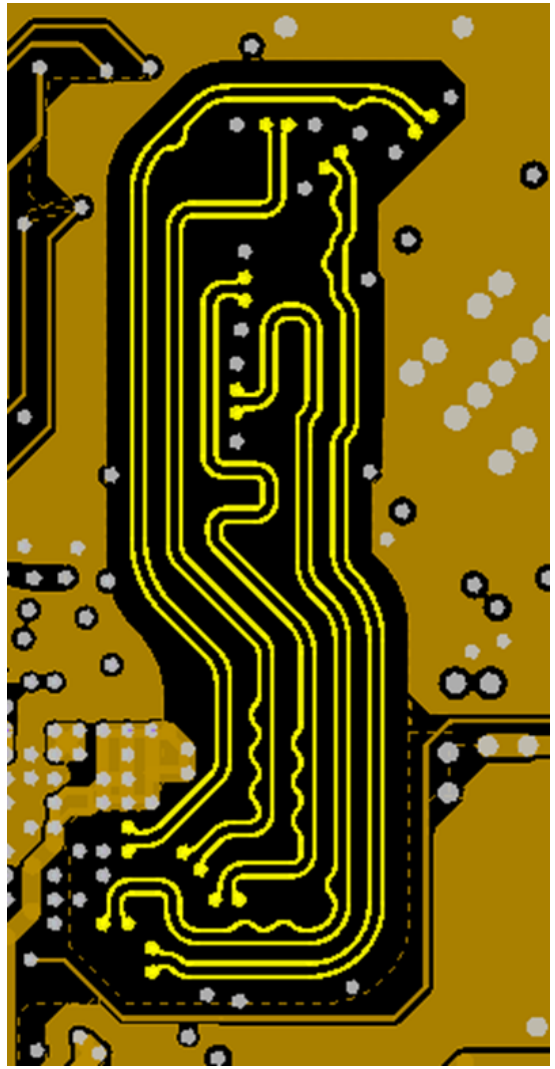


Image Signal Processor

Layout Recommendations (Cont.)

Layer 3 traces has less spacing with GND polygon.

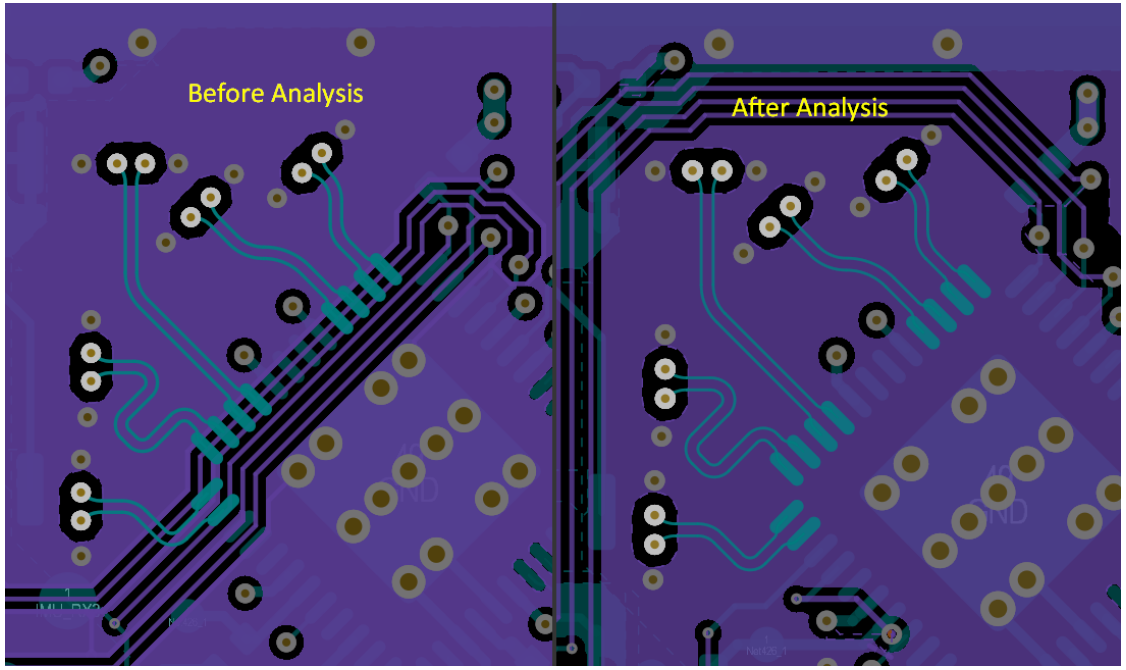
Need to increase spacing. It should be
5H (5 x 6 .9 = 34.5 mils)



Layout Implementations (Cont.)

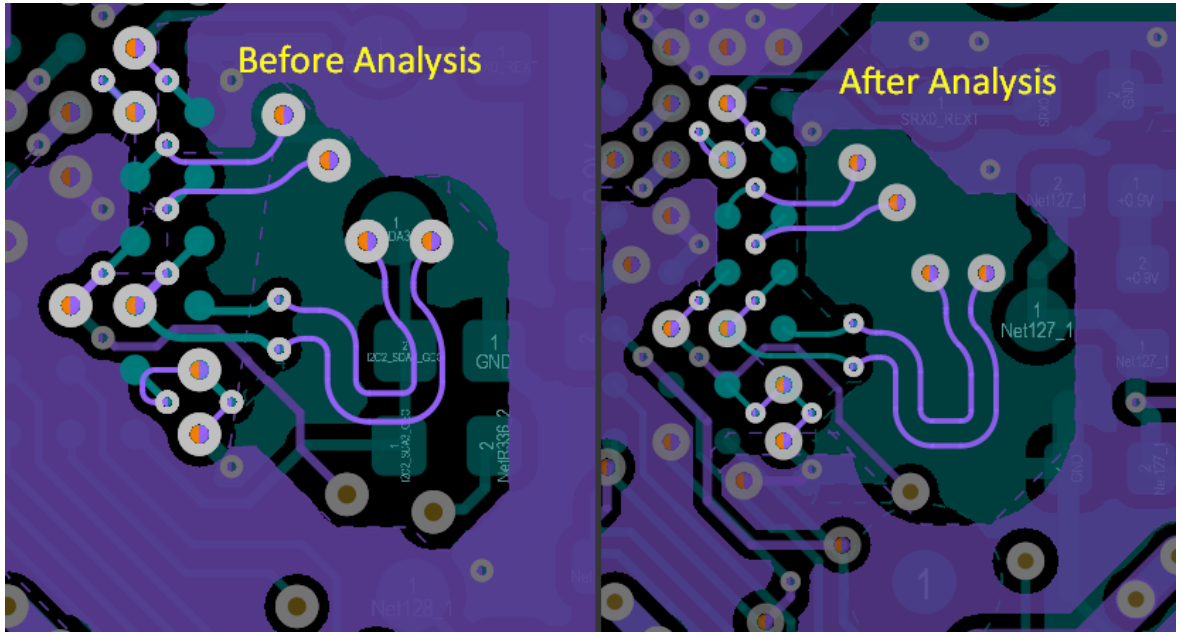
Layer 5:

In Layer 5 routing optimized to provide solid GND reference plane for the Bottom MIPI signal traces and pads.



Layer 6:

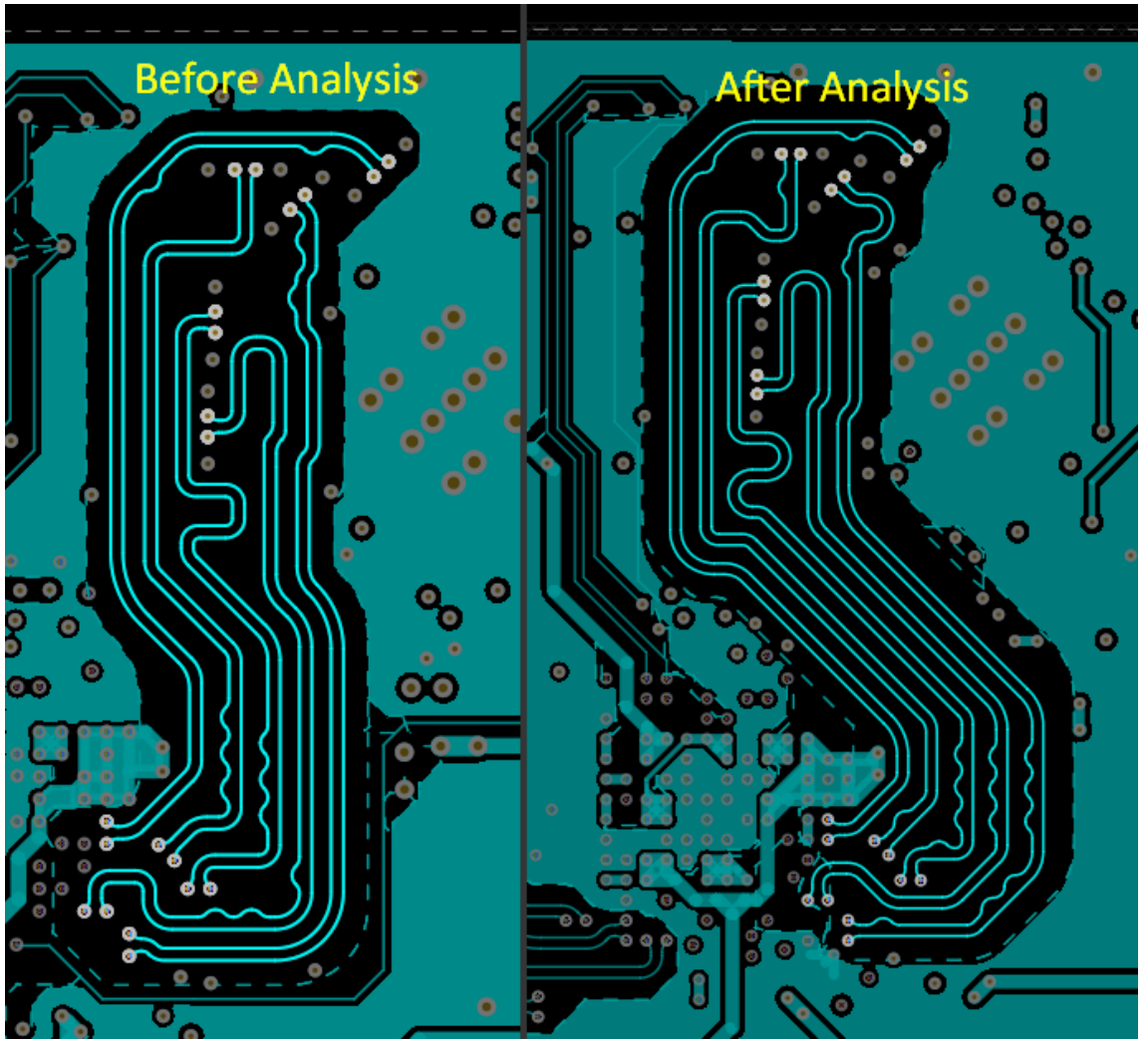
In Layer 6 placement optimized to provide solid GND reference plane for the layer 5 MIPI signal traces.



Layout Implementations (Cont.)

Layer 3:

Routing optimized to increase the spacing (5H - 34.5 mils) between GND and MIPI signal traces.



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Customer Testimonial

Delighted to share a fulfilled client's testimonial that serves as strong evidence of success and impact of the Power Integrity Analysis.

"We requested them to design the project and perform SI analysis to assess the layout's performance, deals with various power circuits and highspeed signals. They not only fulfilled our requirements, went beyond our expectations. They efficiently optimized signal routings along with cost-effective modifications to cu pours, that improved performance, and ensured consistency. The seamless ease updates has resulted in substantial time savings and showcasing an output of exceptional quality. Moreover, their commitment to on-time deliveries has instilled trust in their capability to tackle challenging projects while maintaining top-notch quality."

Conclusion

We provided the client with a list of recommendations to make the signal integrity work better, and implemented the changes in the layout design for boosting the layout's performance. This displayed our strong commitment to delivering high-quality work and our technical expertise.

Our collaboration extends beyond technical aspects; it is about optimizing the signals for better integrity by combining our expertise with a thorough understanding of the client's requirements.

We're dedicated to providing excellent Analysis services, which proves our skill and trustworthiness in achieving outstanding results.