Design & Power Integrity Analysis of Mirror ISP Layout

Scope : Design & PDN Integrity analysis

Application : ADAS - Enhancing Performance of the Layout

Designing a PCB layout encompasses creating layout that aligns with the specified requirements. Power integrity analysis involves analyzing the structure and electrical behavior of the Power Delivery Network (PDN) in a PCB layout.

This includes everything from the power supply, to the routing and vias, the power and ground plane pairs, the capacitors, and of course the devices themselves. The outcome of analysis leads to enhance the performance of the layout significantly and rendering it suitable for application in the field of Autonomous Driver Assistance Systems (ADAS).

Design & Power Integrity Analysis

Challenges

- Fine Pitch BGA- 0.65mm
- Blind Buried Vias
- High Speed signals – MIPI, LVDS
- Multiple Power Pours
- Voltage Drop, Current Density & Via Current
  (Parameters mentioned for respective powers in the Analysis slides)
- PDN Impedance (Z) parameters
- Frequencies Outages to Reduce High-Z
- Internal resistance of power planes
- Power rail – Ripple & Noise coupling

Requirements

- Fine-Tune Component Placement
- Keep things separate – Power & HS Signals
- Ensure clean power
- Minimize power loss
- Minimize Thermal & Electromagnetic interaction
- High Z- reductions
- Choice of de-caps and placement
- Performance enhancement

Layout Design & PI Analysis - SoW

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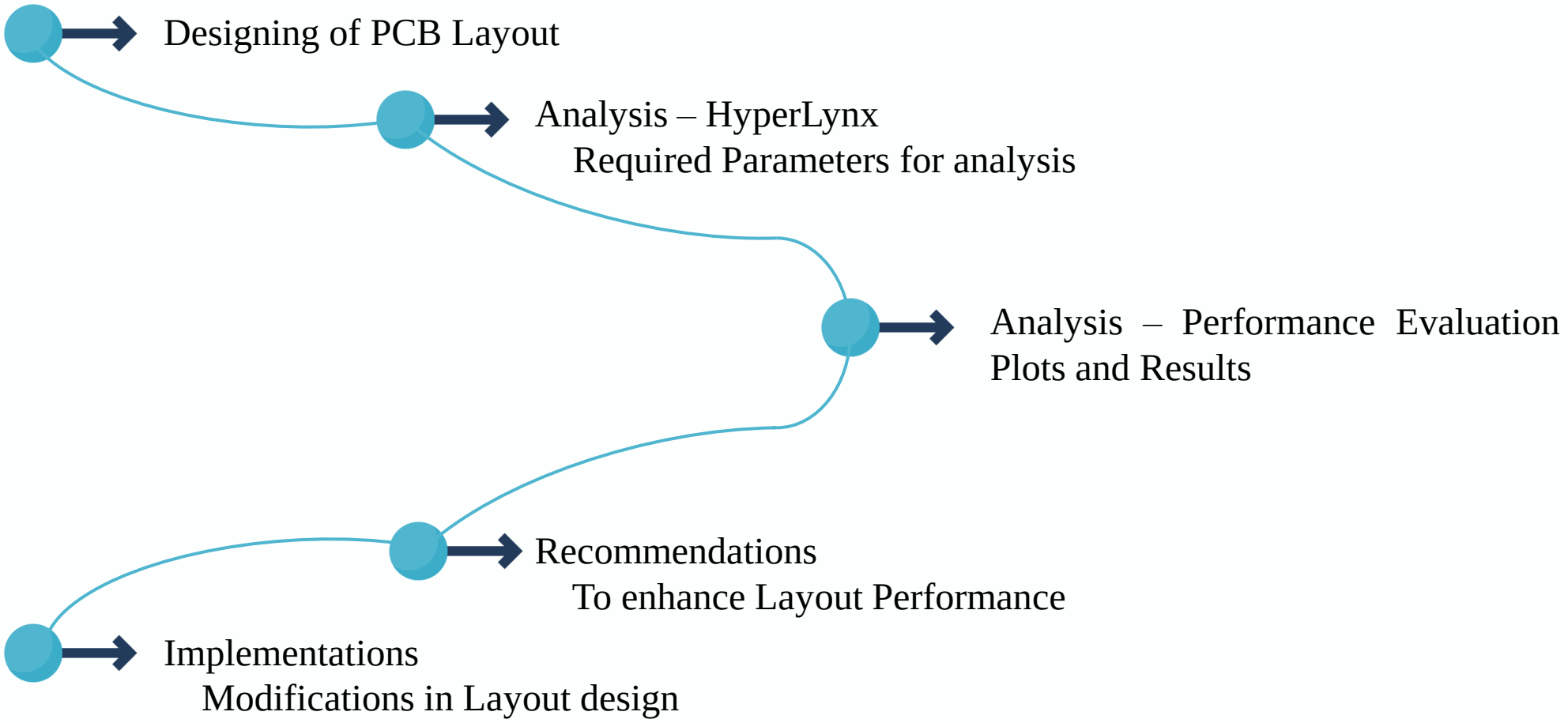

Design of PCB Layout – How we executed?

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This layout includes circuits like De-Serializer, Image Signal Processor, and Display Controller. They work together for the TFT Display, showing the signals from the camera in an Autonomous application. The Layout design is completed based on the instructions and requirements from the client.

Power Circuits

- +12V
- SEPIC Power – 9.5V
- Coax Power – 8.6V
- +3.3V
- +5V
- +2.0V
- +1.8V
- +1.5V
- +0.9V

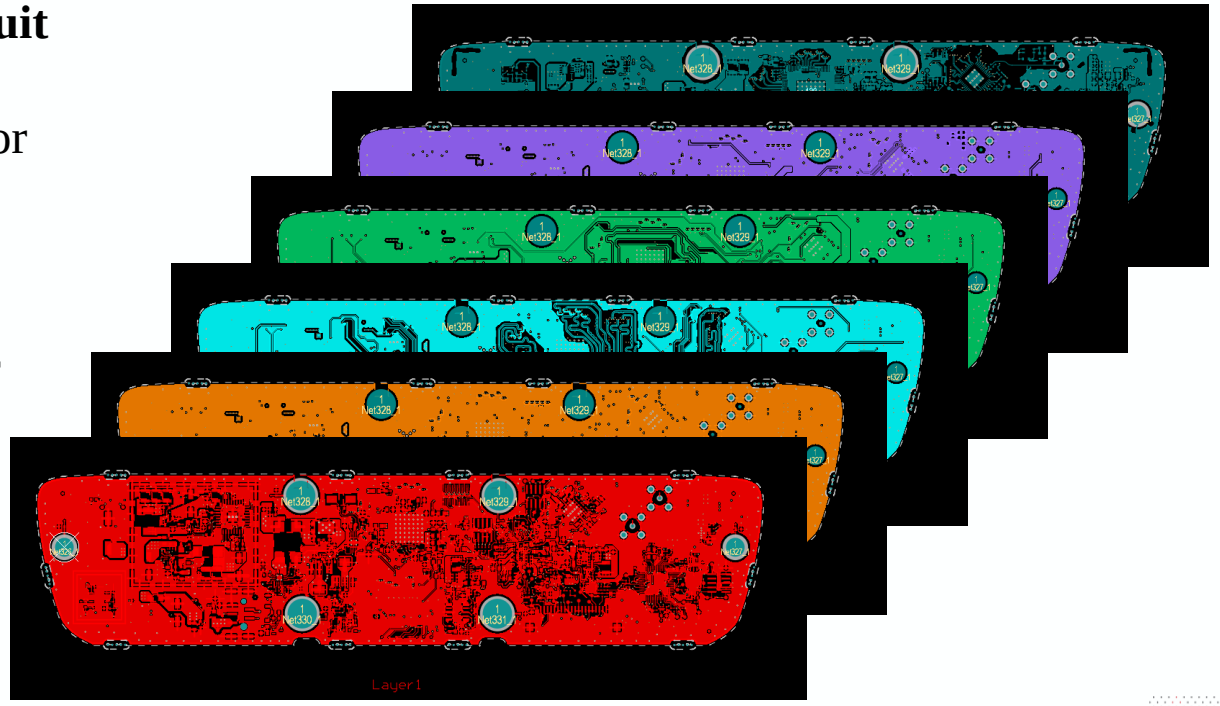
High Speed Signal Circuit

- De-serializer
- Image Signal Processor
- Display Controller

Sensor Circuit

- Ambient Light Sensor
- Toggle sensor

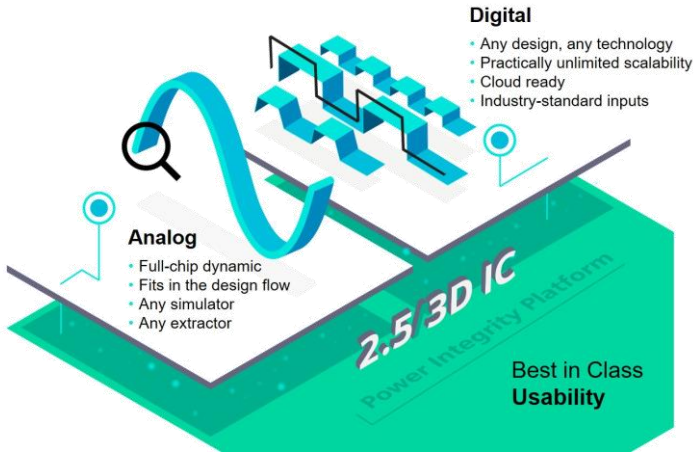
Finished Layout



*The finished layout design file needs to be analyzed to assess its performance.

Analysis – How we executed?

We executed the analysis in **HyperLynx** tool, to evaluate the power integrity performance of the layout.

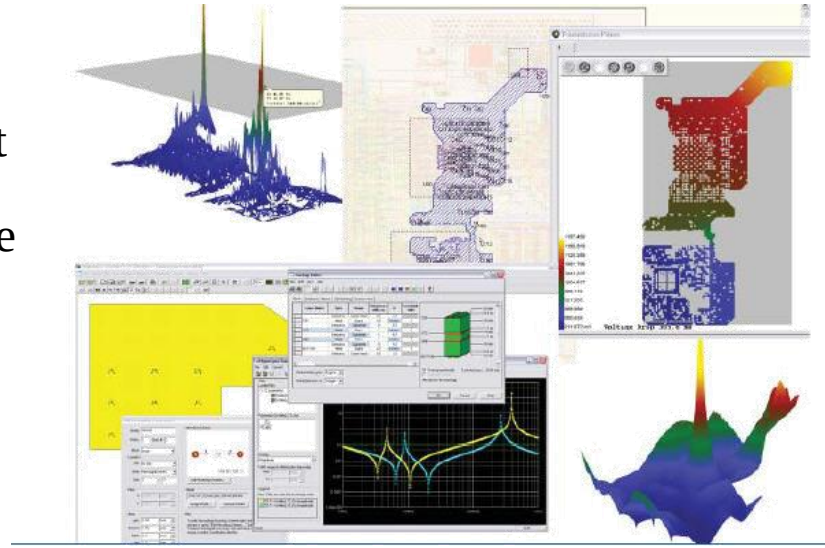


Power integrity analysis aims to identify operation problems from two perspectives: DC (IR Drop) and AC (Frequency)

Quantities to calculate include:

- ✓ DC resistance and current density in rails and planes
- ✓ Voltage and current distribution throughout the PCB layout
- ✓ Transient response on power rails observed in the time domain

$$Z(\omega) = \frac{V_{\text{core}} \times V_{\text{ripple}}(\%)}{I_{\text{chip}}(\omega) + I_{\text{DC}}}$$

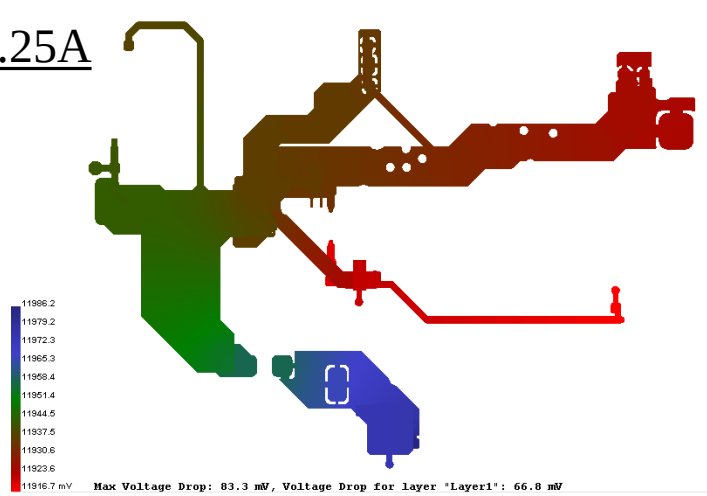


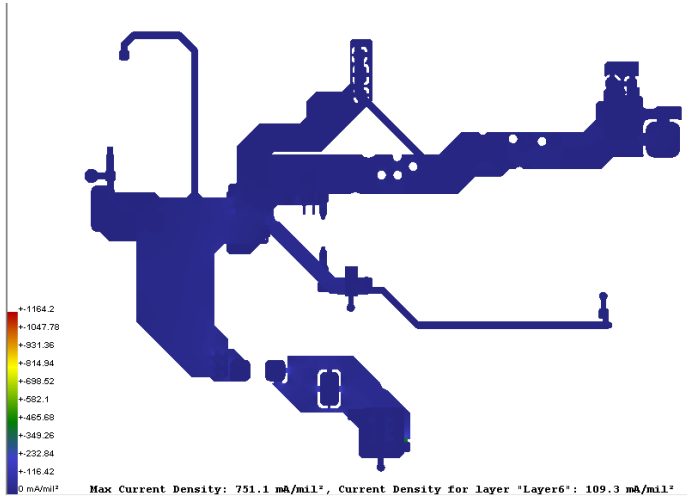
Analysis – Plots and Results (Cont.)

Voltage Drop

Current Density

Net Name: +12V Voltage:12V Current:3.25A





Analysis Parameters – Requirements

Max. Voltage Drop – 5.00%

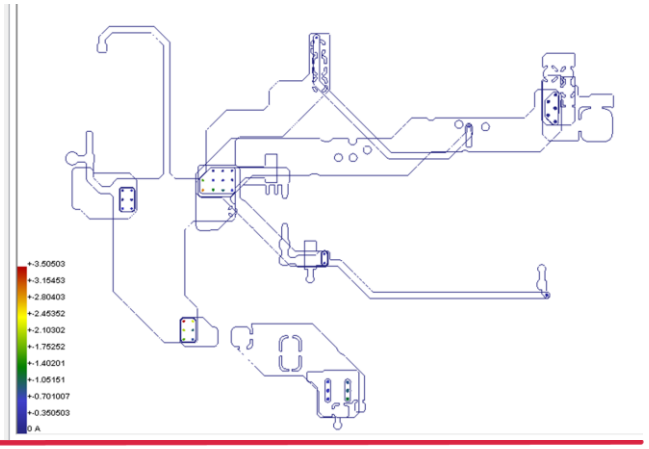
Max. Current Density – 100.00mA/mil²

Max. Via Current – 1000.0mA

Analysis Result

#	Measurement	Test	Constraint	Max Value	Location
	Filter	Filter	Filter	Filter	Filter
1	Max Voltage Drop	PASS	5.000%	NET +12V: 0.694% (83.3mV)	pin TP119.1
2	Max Current Density	FAIL	100.00mA/mil2	751.10mA/mil2	(12.575, 17.287), layer Layer1
3	Max Via Current	FAIL	1000.0mA	3505.0mA	(11.915, 17.588) between layers Layer5 and Layer6

Via Current



Analysis – Plots and Results (Cont.)

Net Name: +9.5V Voltage:9.5V Current:0.55A

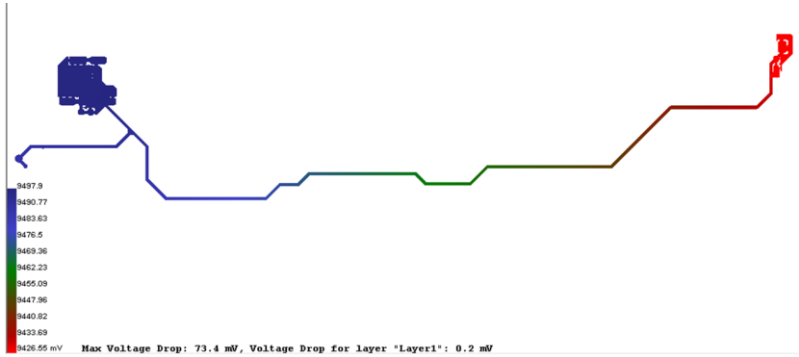
Analysis Parameters – Requirements

Max. Voltage Drop – 5.00%

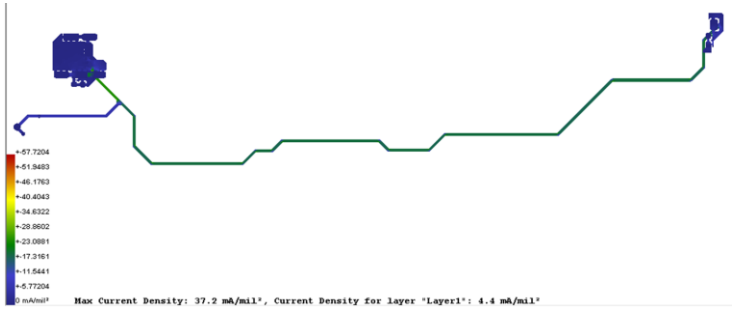
Max. Current Density – 50.00mA/mil²

Max. Via Current – 1000.0mA

Voltage Drop



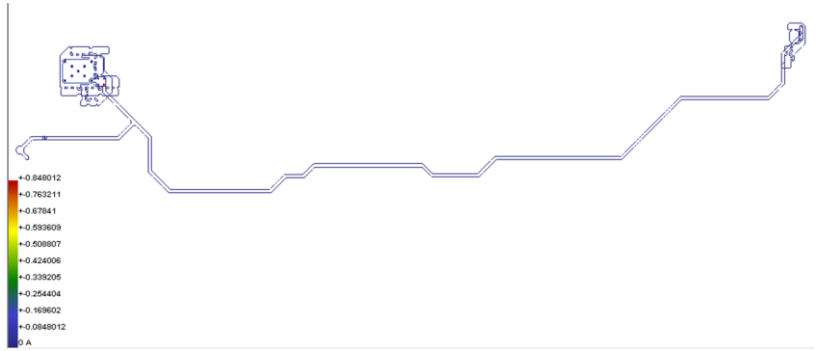
Current Density



Analysis Result

#	Measurement	Test	Constraint	Max Value	Location
	Filter	Filter	Filter	Filter	Filter
1	Max Voltage Drop	PASS	5.000%	**NET 9.5V: 0.773% (73.4mV)**	pin U110.1
2	Max Current Density	PASS	50.00mA/mil2	**37.24mA/mil2**	(14.190, 18.202), layer Layer5
3	Max Via Current	PASS	1000.0mA	**848.0mA**	(14.180, 18.241) between layers Layer5 and Layer6

Via Current



Analysis – Plots and Results (Cont.)

Net Name: +3.3V Voltage:3.3V Current:9.53A

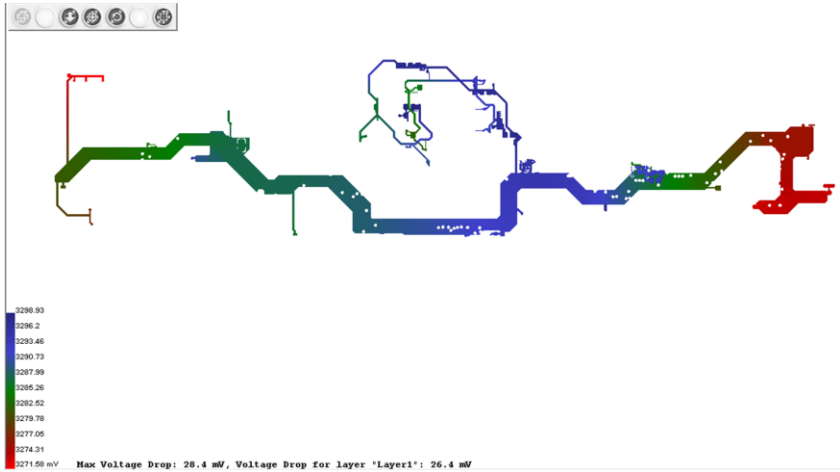
Analysis Parameters – Requirements

Max. Voltage Drop – 5.00%

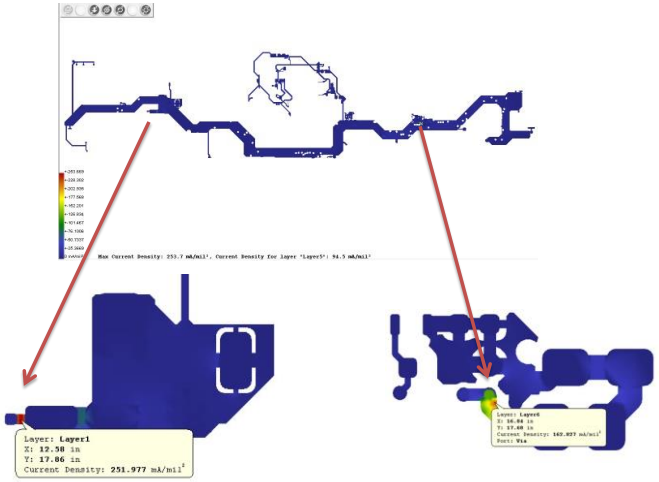
Max. Current Density – 100.00mA/mil²

Max. Via Current – 1000.0mA

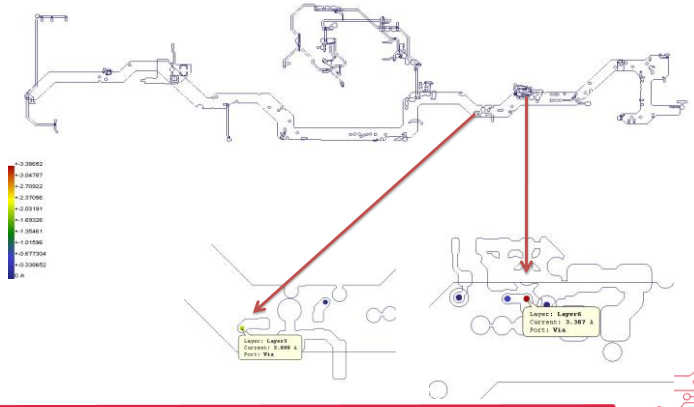
Voltage Drop



Current Density



Via Current

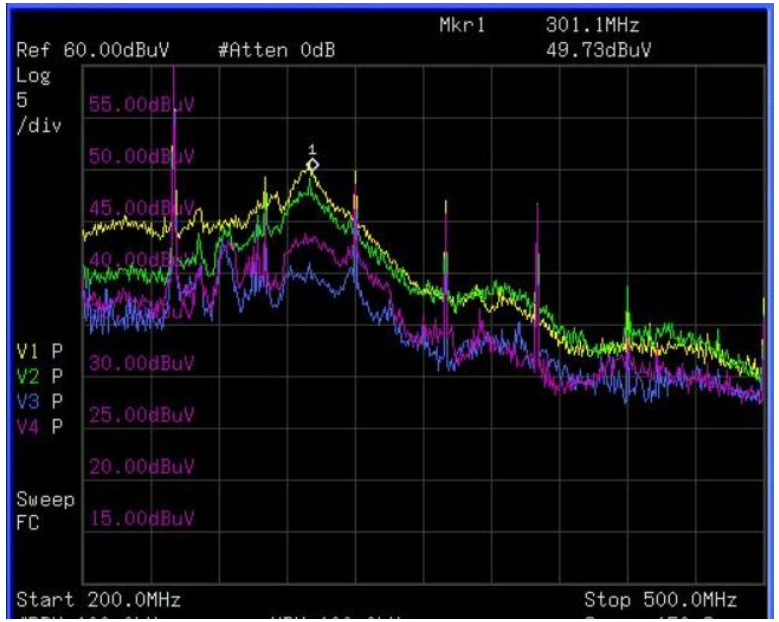


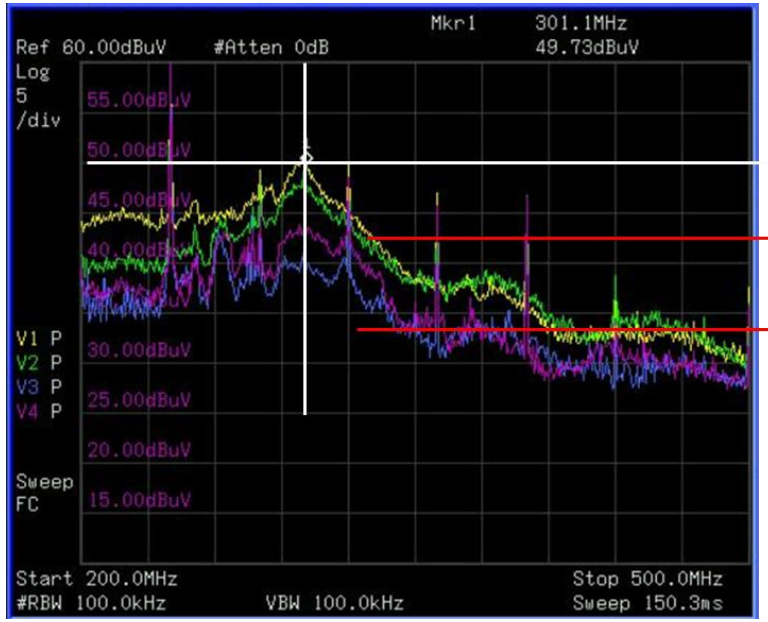
Analysis Result

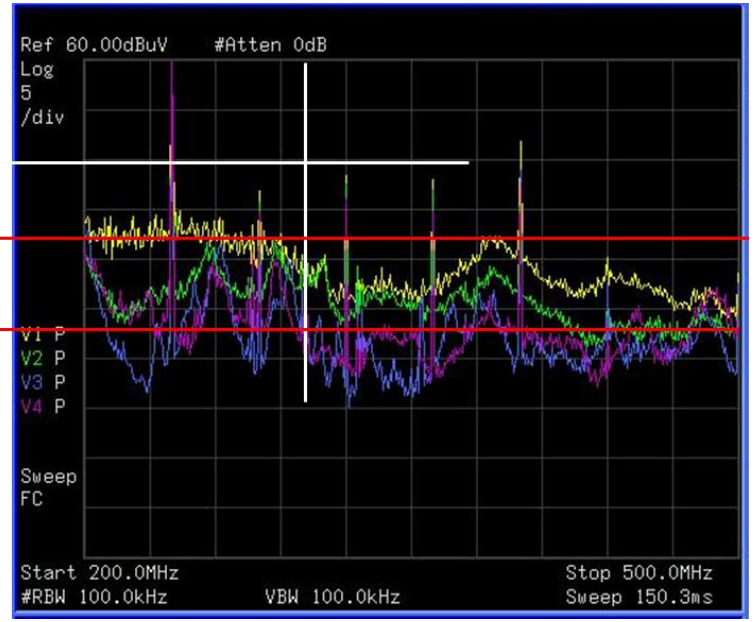
#	Measurement	Test	Constraint	Max Value	Location
	Filter	Filter	Filter	Filter	Filter
1	Max Voltage Drop	PASS	5.000%	**NET +3.3V: 0.861% (28.4mV)**	pin R322.1
2	Max Current Density	FAIL	100.00mA/mil2	**253.67mA/mil2**	(12.584, 17.850), layer Layer1
3	Max Via Current	FAIL	1000.0mA	**3386.5mA**	(16.831, 17.691) between layers Layer5 and Layer6

Analysis – Plots and Results (Cont.)

High-Z probe measurements - Frequency Range 200MHz – 500MHz.







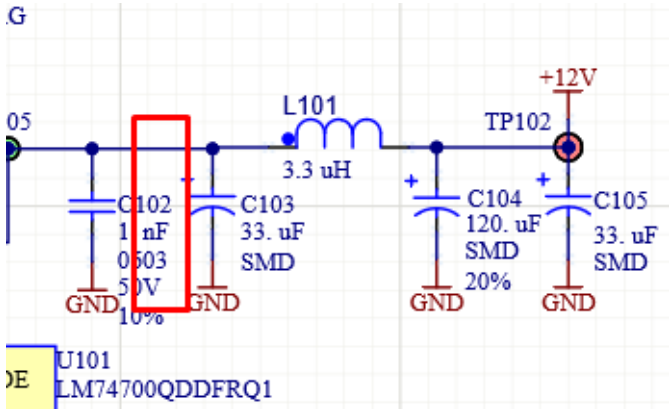
Recommendation - Adding new cap 1 uF at input filter section reduced the 300 MHz peak ≈ 10 dB.

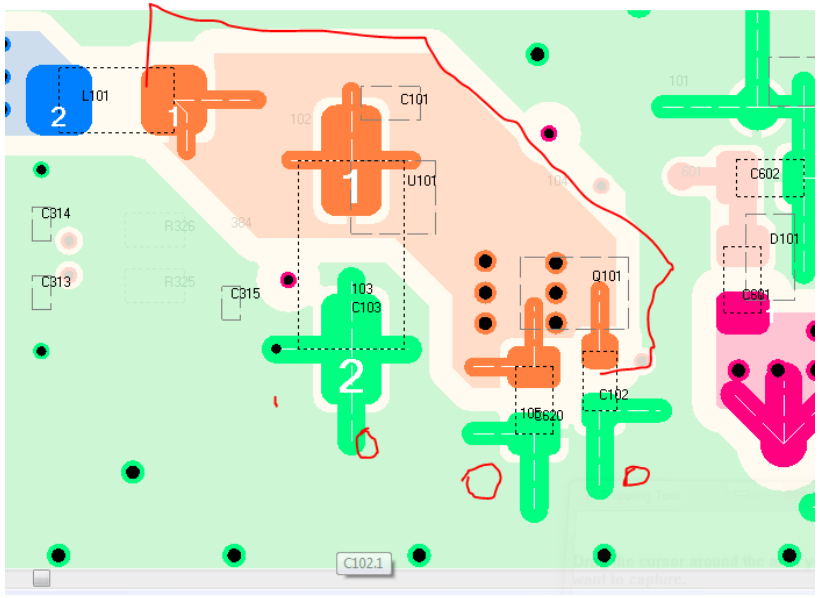
Layout Recommendations (Cont.)

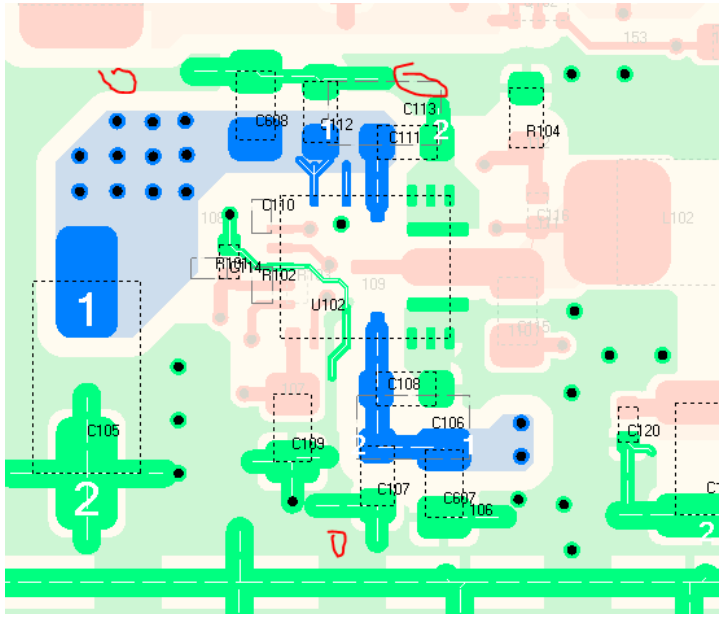
+12V layout recommendations:

1. Add cap (1uF) in the input filter section to reduce the high Z noise.

2. Increase the width of Cu pour and Add GND vias at the specified locations.



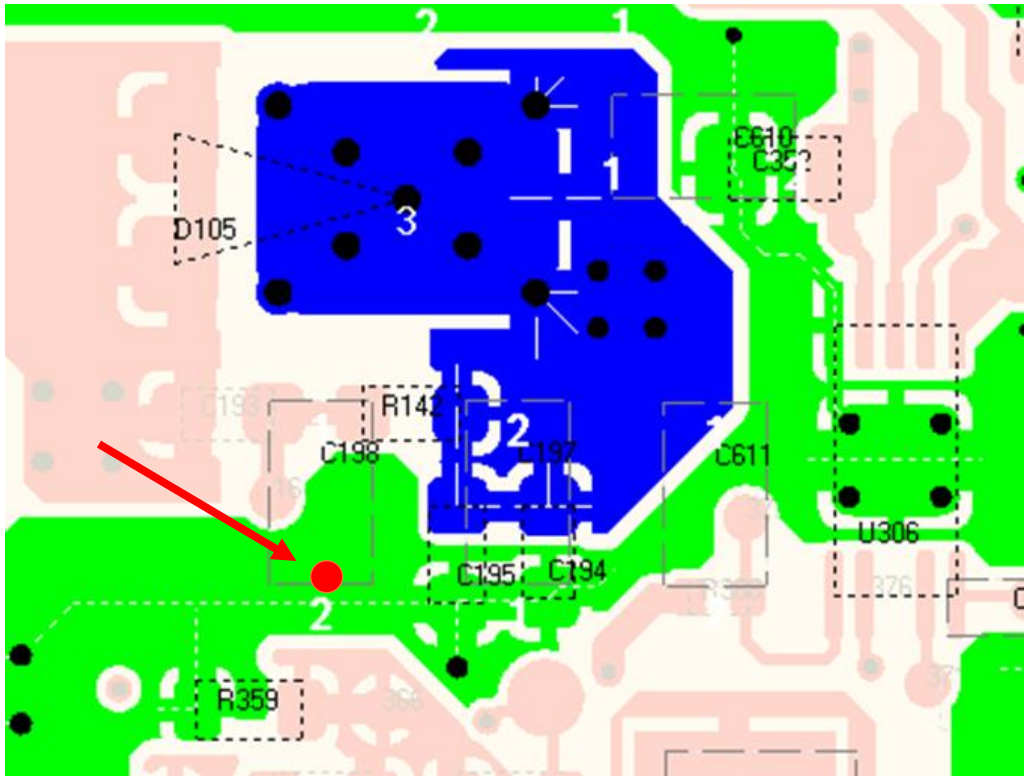




Layout Recommendations (Cont.)

+9.5V layout recommendations:

1. Increase the routing trace width and optimize the routing path.
2. Add GND via.



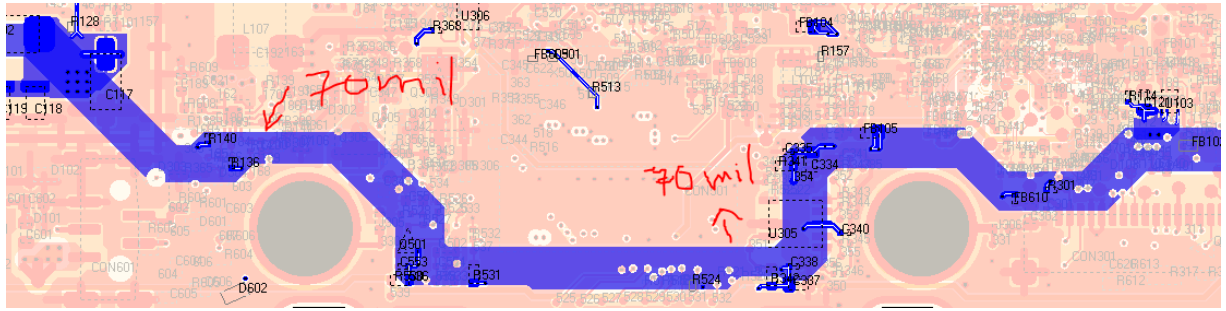
Layout Recommendations (Cont.)

+3.3V layout recommendations:

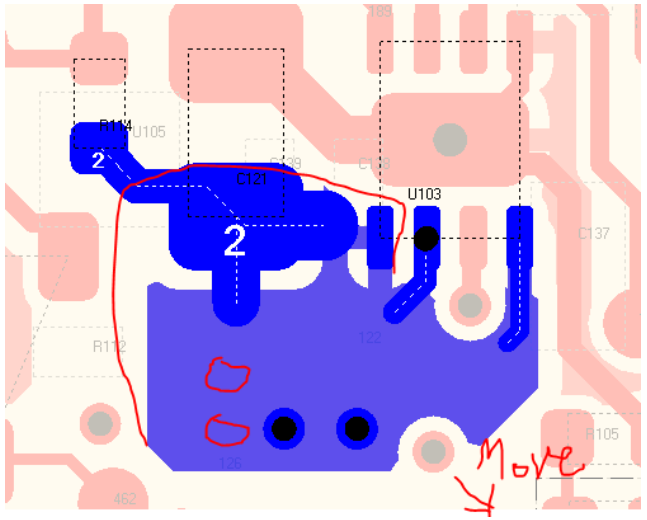
1. Increase the width of the Cu pour at specified area.

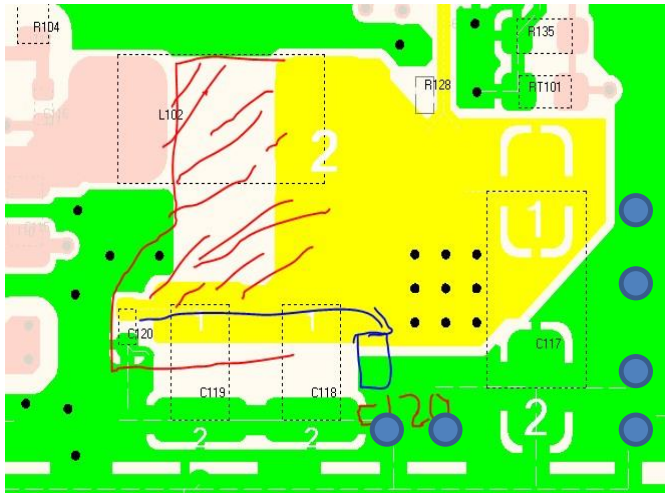
2. Modify C120 placement and add return GND vias at the specified locations.

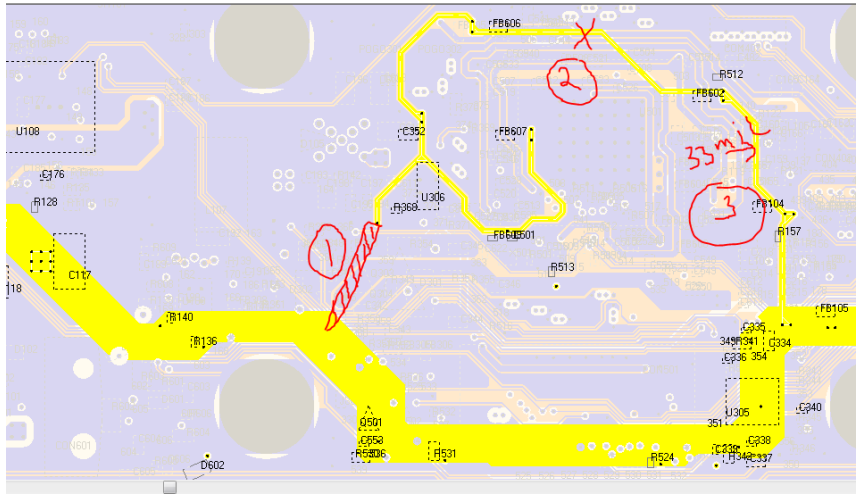
Layer 5



Top Layer





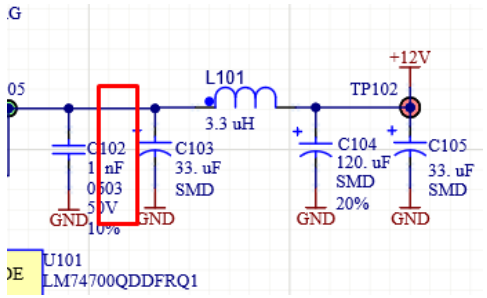


Layout Implementations (Cont.)

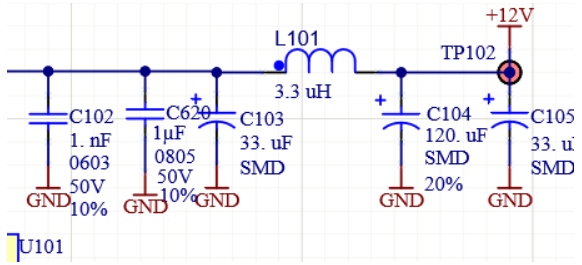
+12V layout Implementation:

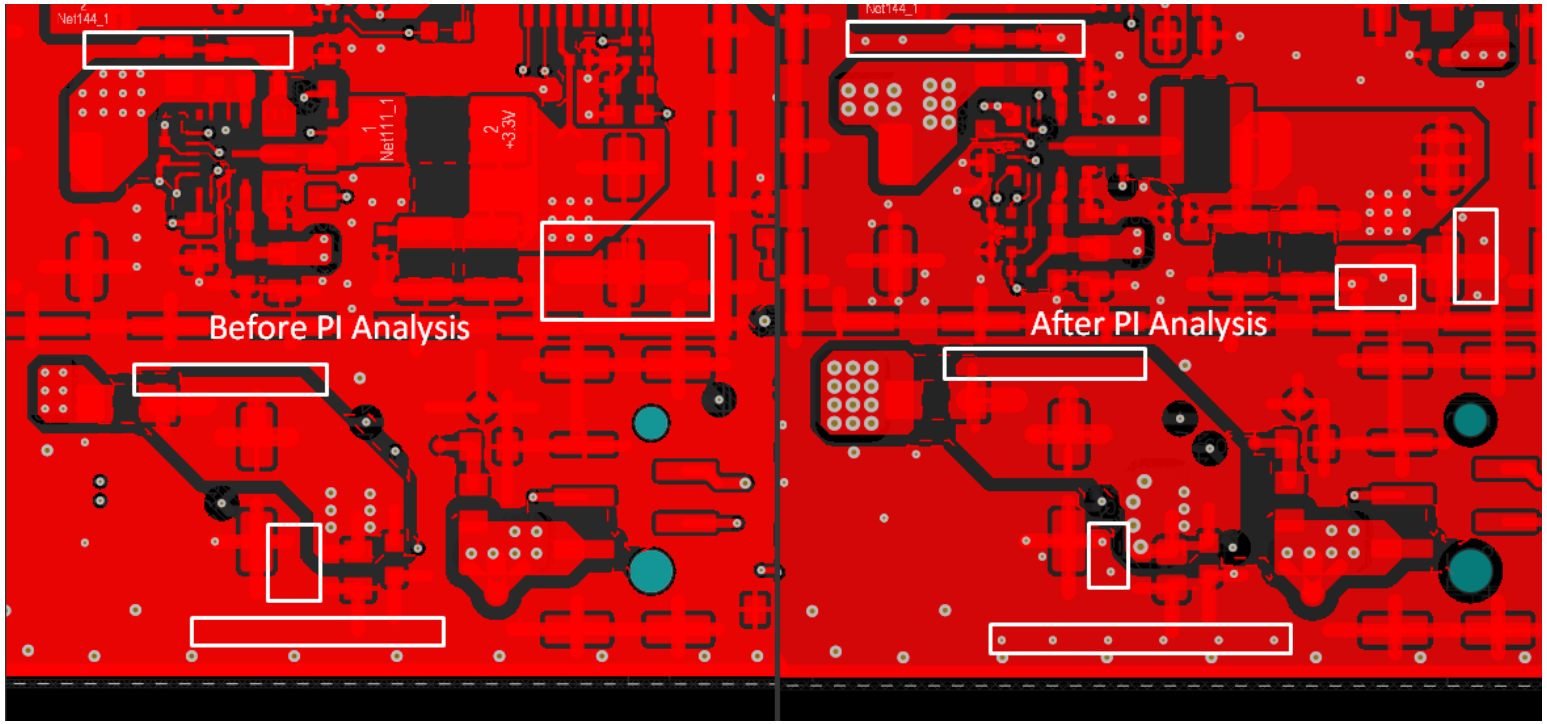
1. Added new cap (1uF – C620).
2. Increased the width of Cu pour and GND vias added.

Before



After

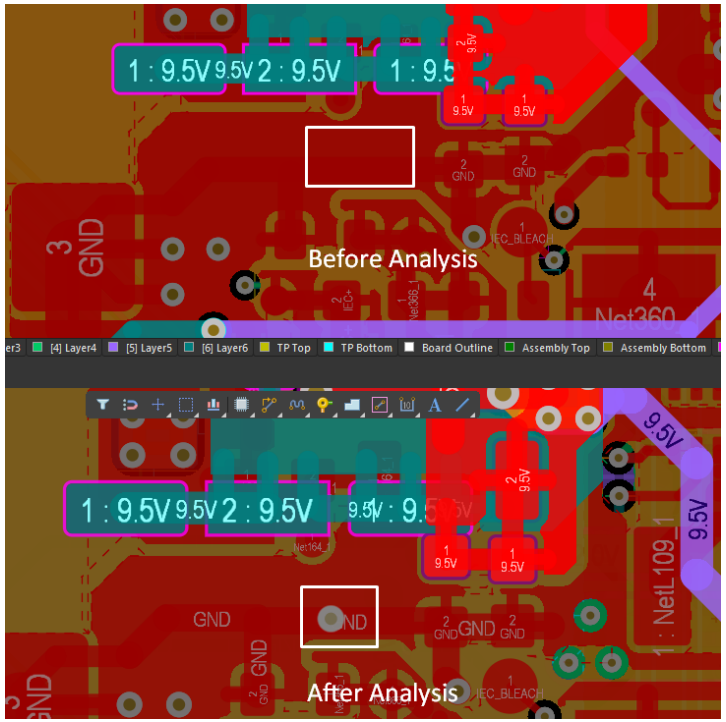




Layout Implementations (Cont.)

+9.5V layout Implementation:

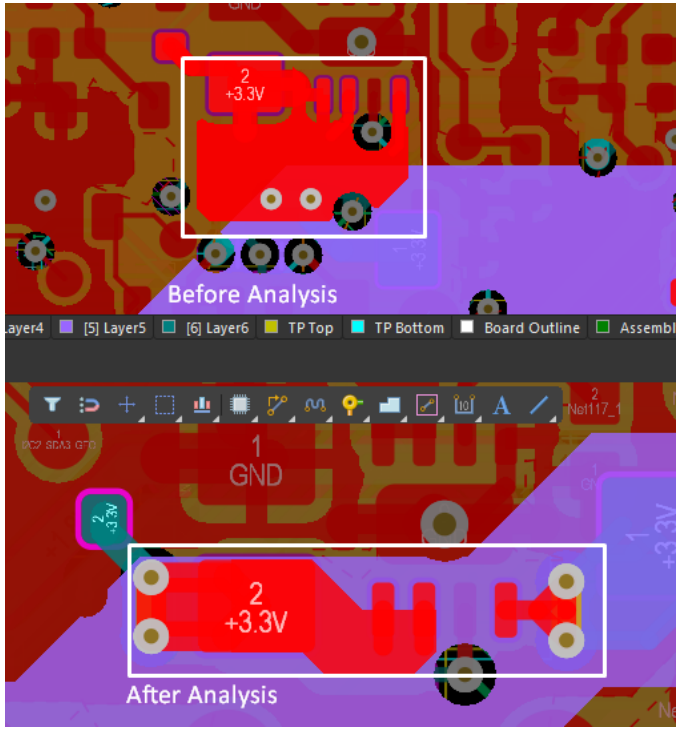
1. Routing trace width increased and routing path optimized.
2. GND Vias added.



Layout Implementations (Cont.)

+3.3V layout Implementation:

1. Increased the width of Cu pour and routing optimized.
2. Polygon optimized and Vias added.



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Customer Testimonial

Delighted to share a fulfilled client's testimonial that serves as strong evidence of success and impact of the Power Integrity Analysis.

"We requested them to design the project and perform PI analysis to assess the layout's performance, deals with various power circuits and highspeed signals. They not only fulfilled our requirements, went beyond our expectations. They efficiently optimized our power circuits along with cost-effective modifications to cu pours, that improved performance, and ensured consistency. The seamless ease updates to the power circuits has resulted in substantial time savings and showcasing an output of exceptional quality. Moreover, their commitment to on-time deliveries has instilled trust in their capability to tackle challenging projects while maintaining top-notch quality."

Conclusion

We provided the client with a list of recommendations to make the power delivery network work better, and implemented the changes in the layout design for boosting the layout's performance. This displayed our strong commitment to delivering high-quality work and our technical expertise.

Our collaboration extends beyond technical aspects; it is about optimizing the PDN by combining our expertise with a thorough understanding of the client's requirements.

We're dedicated to providing excellent Analysis services, which proves our skill and trustworthiness in achieving outstanding results.