Restart and Trunk Circuit Modification Design

Scope: Hardware Design

Application: Battery Management System (BMS)

When it comes to keeping rechargeable batteries in check, the hardware circuit design of a Battery Management System (BMS) is key. This circuit is like the brain of electric vehicles, making sure everything runs smoothly. In our Restart and Trunk section, the hardware circuit design is crucial. It's responsible for detecting press signals accurately while filtering out sudden noise to avoid unintended actions during specific programmed tasks.

Hardware Design – Challenge

The client encountered a challenge with the functionality of the existing circuit design. Specifically, the BMS module on SBC1 had not meet the below updated requirements.

Challenge:

Wake up recognition:

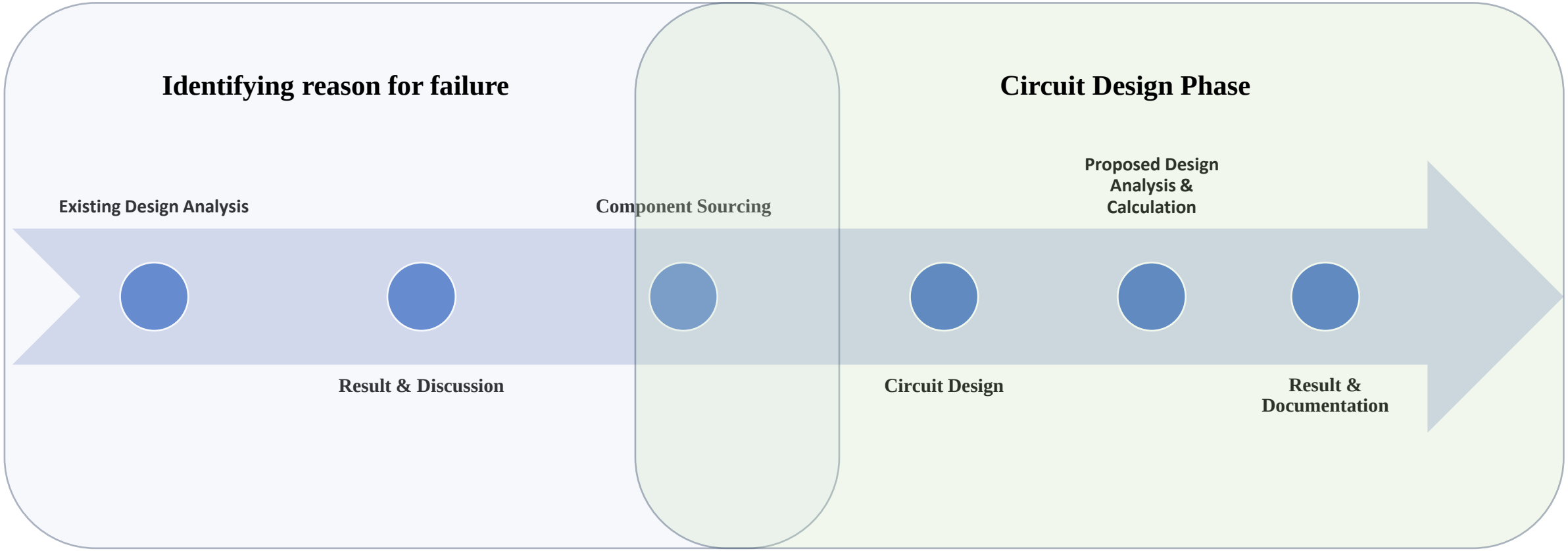
For Restart,

- At least right before 8V@100ms, it is recognized as High and Wake up is required
- Wake up recognition circuit design
- ① Implementation of latch circuit for pulse input signal
- ② Digital input for the signal at the end of the latch circuit

For Trunk,

- Recognize as LOW from a minimum value of 2.2V or higher and require Wake Up
- Recognize only pulse signals longer than 20ms
- ① Implementation of latch circuit for pulse input signal
- ② Digital input for the signal at the end of the latch circuit

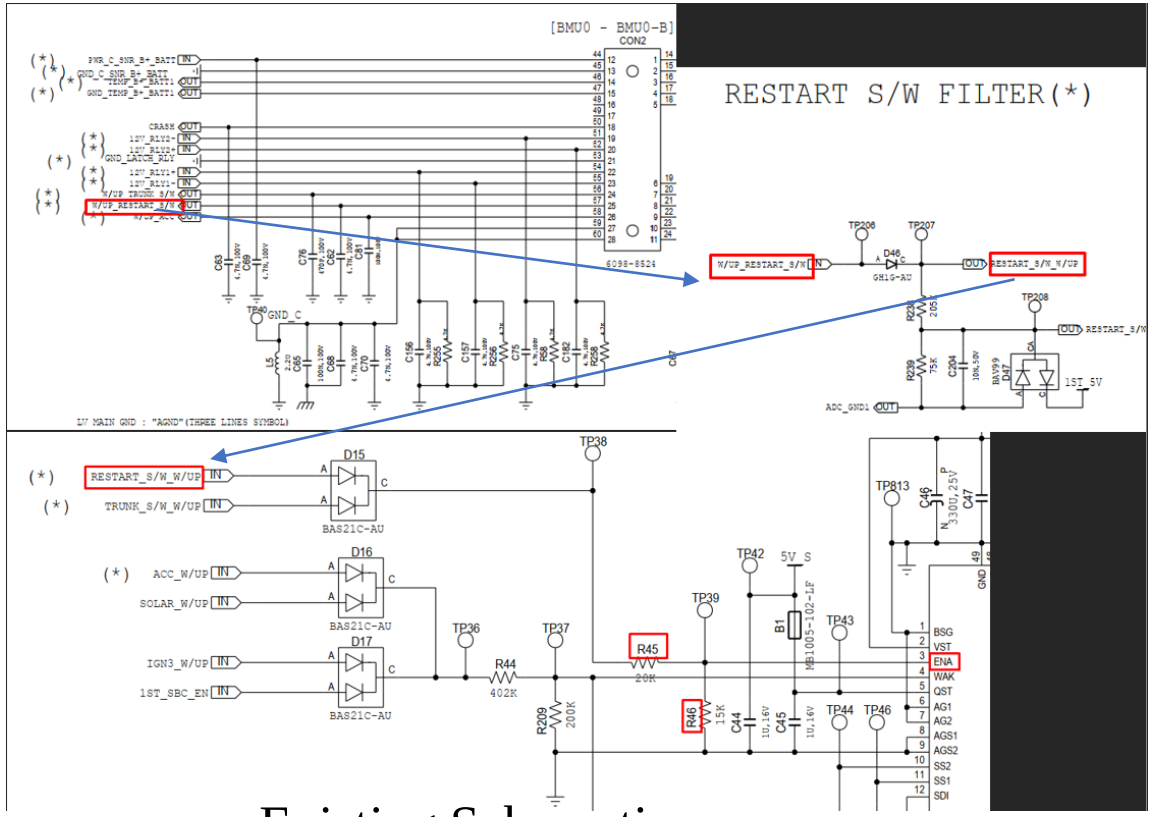
Hardware Design – SoW



Every stages of work have multiple brainstorming and review with the client

Identifying reason for failure

Existing Design Analysis



Existing Schematic

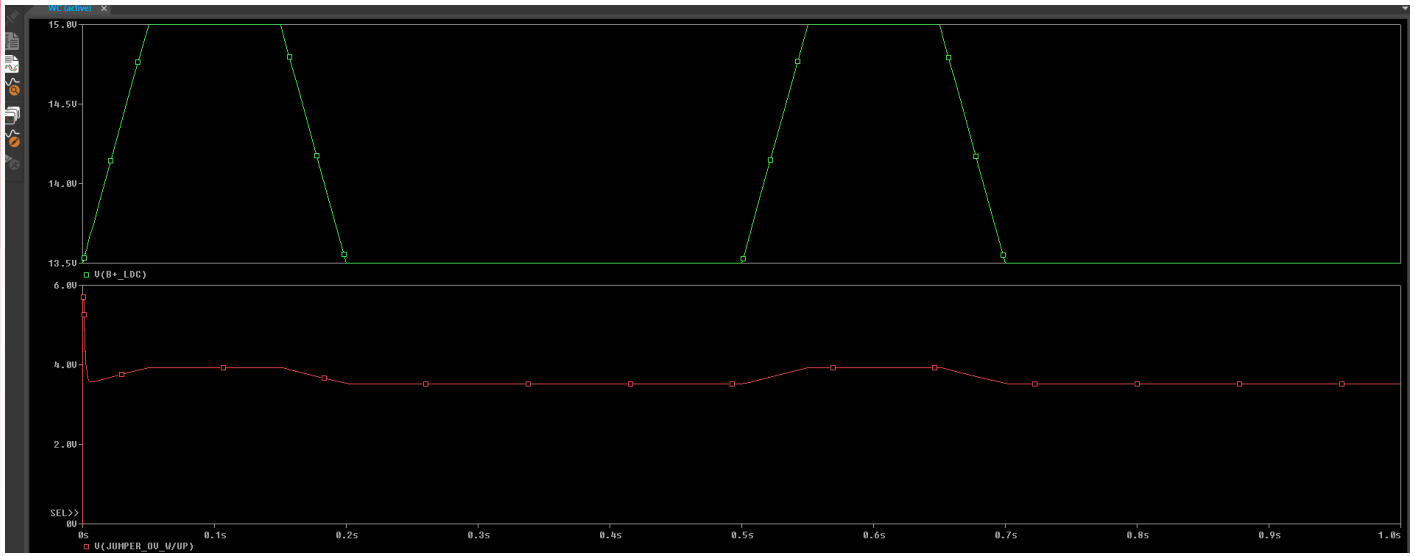
Working:

Existing Circuit Design consist a set of discrete components to reduce the voltage that can be used by the pin of SBC1.

Then, the SBC1 is programmed to monitor the voltage without introducing any delay.

Identifying reason for failure

Result & Discussion



According to a study on existing circuit design, it has been concluded that the SBC1 is unable to create a delay when the input signal is analog and experiences a sudden rise in voltage.

Component Sourcing

We sourced TI, Analog Devices and RoHM for component.

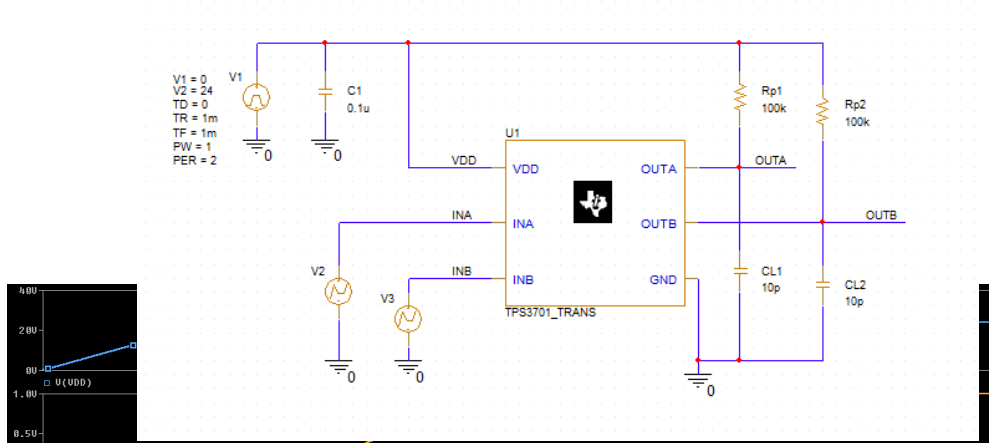
In that Analog Devices and RoHM don't have ability to detect above 6V but TI's TPS37-Q1 has the internal voltage divider configuration to detect the exact voltage that we need with dual Adjustable time Delay.

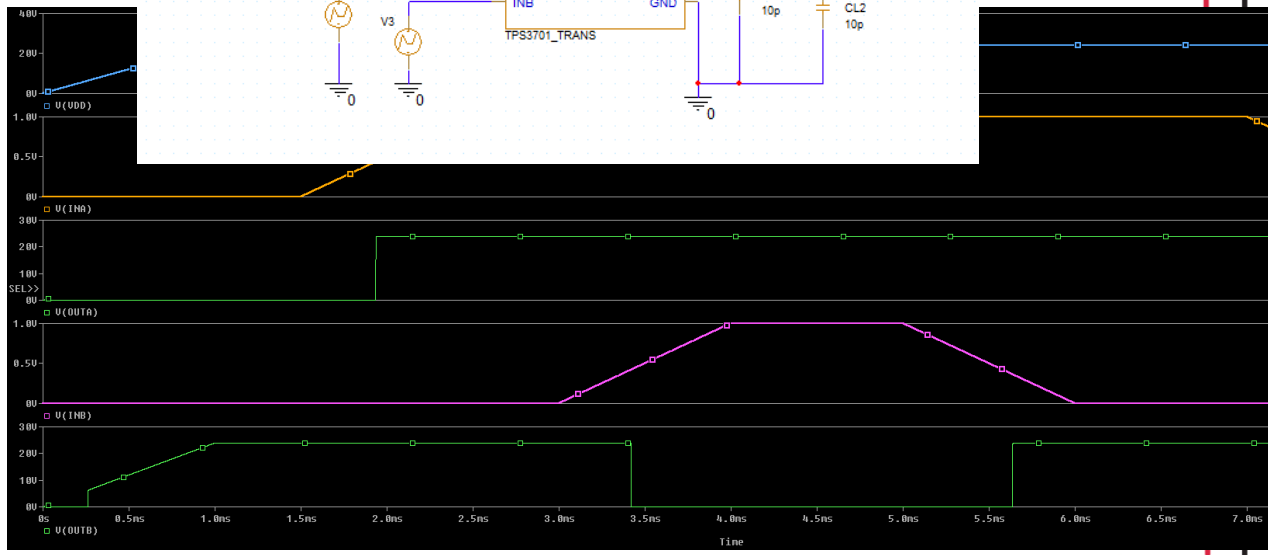
Circuit Design Phase

Proposed Circuit Design

- Circuit with the TPS37x chip generates the RESET when the voltage level is from 8V @ 100 mS, and the circuit functionality on SBC1 is meeting RESTART wakeup detection as per the requirement.
- The Latch is reset back by the GPIO signal from the MCU1-RESTART_LATCH
- Circuit with the TPS37x chip generates the RESET when the voltage level is higher from 2.2V @ 20 mS, and the circuit functionality on SBC1 is meeting TRUNK wakeup detection as per the Requirement.
- The Latch is reset back by the GPIO signal from the MCU1-TRUNK_LATCH

Created a rough schematic to rough analysis to check the requirement and done an analysis to verify.





Circuit Design Phase

Proposed Design Calculations

Timing Calculation

$t_{CTSx\ (typ)} = -\ln(0.28) \times R_{CTSx\ (typ)} \times C_{CTSx\_EXT\ (typ)} + t_{CTSx\ (no\ cap)}$

R_{CTSx} = is in kilo ohms (kOhms)

C_{CTSX_EXT} = is given in microfarads (µF)

t_{CTSx} = is the sense time delay (ms)

$t_{CTSx\ (min)} = -\ln(0.31) \times R_{CTSx\ (min)} \times C_{CTSx\_EXT\ (min)} + t_{CTSx\ (no\ cap\ (min))}$

$t_{CTRx\ (max)} = -\ln(0.25) \times R_{CTSx\ (max)} \times C_{CTSx\_EXT\ (max)} + t_{CTSx\ (no\ cap\ (max))}$

Delay Timing Calculation

=(B7-B4)/(-LN(0.28)*B1)

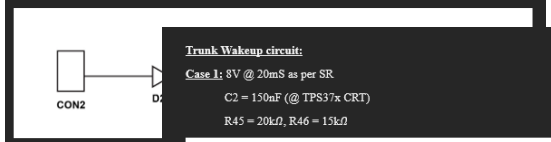
	A	B	C	D	E
1	Rcts(typ)(kΩ)	100			
2	Rcts(min)(kΩ)	88			
3	Rcts(max)(kΩ)	122			
4	Tcts(typ)(ms) no cap	0.008			
5	Tcts(min)(ms) no cap	0.008			
6	Tcts(max)(ms) no cap	0.017			
7	Tcts(typ)(ms) desired	20	input		
8	Cctr(typ)(µF) desired	0.16	input	cap tolerance(%)	10
9					
10	Cctr(typ)(µF) calculated	=(B7-B4)/(-LN(0.28)*B1)			
11					
12	Tcts(typ)(ms) calculated	20.37545			
13	Tcts(min)(ms)	14.84923			
14	Tcts(max) (ms)	29.78351			

Restart Wakeup Circuit:

Case 1: 8V @ 100ms as per SR

C3=800nF (@ TPS37x Circuit)

R45 = 20kΩ, R46 = 15kΩ



With given Voltage of 8V:

@ U21 - Sense1

V_{sense1}=8V=0

@ U21 - $\overline{RST1}$

V_{RST1}=8.7V

R46/R45 Voltage Div

$V_{R46} = V_{RST1}$-

= 8.7-0.

= 8.16V

= 8.16V

= 8.16

V_{R46} = 3.5V

@ SBC1:

V_{ENA} = 3.5 (1

= 3.5 (

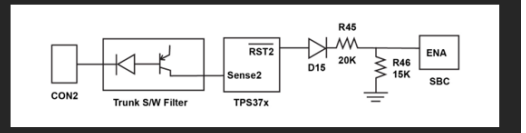
V_{ENA} = 3.34V

Trunk Wakeup circuit:

Case 1: 8V @ 20mS as per SR

C2 = 150nF (@ TPS37x CRT)

R45 = 20kΩ, R46 = 15kΩ



With given voltage of 8V:

@ U21 – Sense2

V_{SENSE2} = 8V

@U21 – $\overline{RST2}$

V_{RST2} = 8.5V

@ R46/R45 Voltage divider

$V_{R46} = V\overline{RST2}$ -0.6

= 8.5-0.6

= 7.9V

$= 7.9 \times \frac{R46}{R45+R46}$

$= 7.9 \times \frac{15k}{35k}$

V_{R46} = 3.39V

@ SBC1

$V_{ENA} = 3.39\ (1 - e^{-t/\tau})$ t = 20.72mS @ nominal condition

$= 3.39\ (1 - e^{-20.72/22.5})$

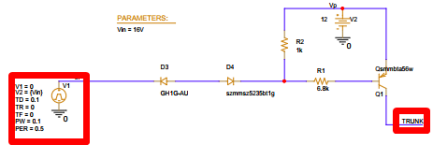
V_{ENA} = 1.565V

Voltage Calculation

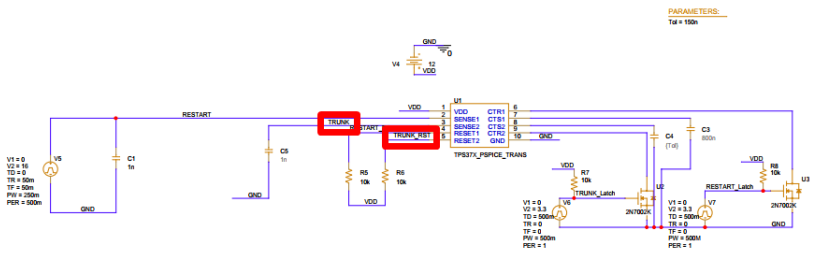
Proposed Design Analysis Setup

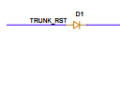
The analysis done by simulating the circuit in 3 different voltages (8V, 9V and 16V) with same delay configuration in IC.

Circuit



From LV Connector





SBC ENA Pin

Circuit Design Phase

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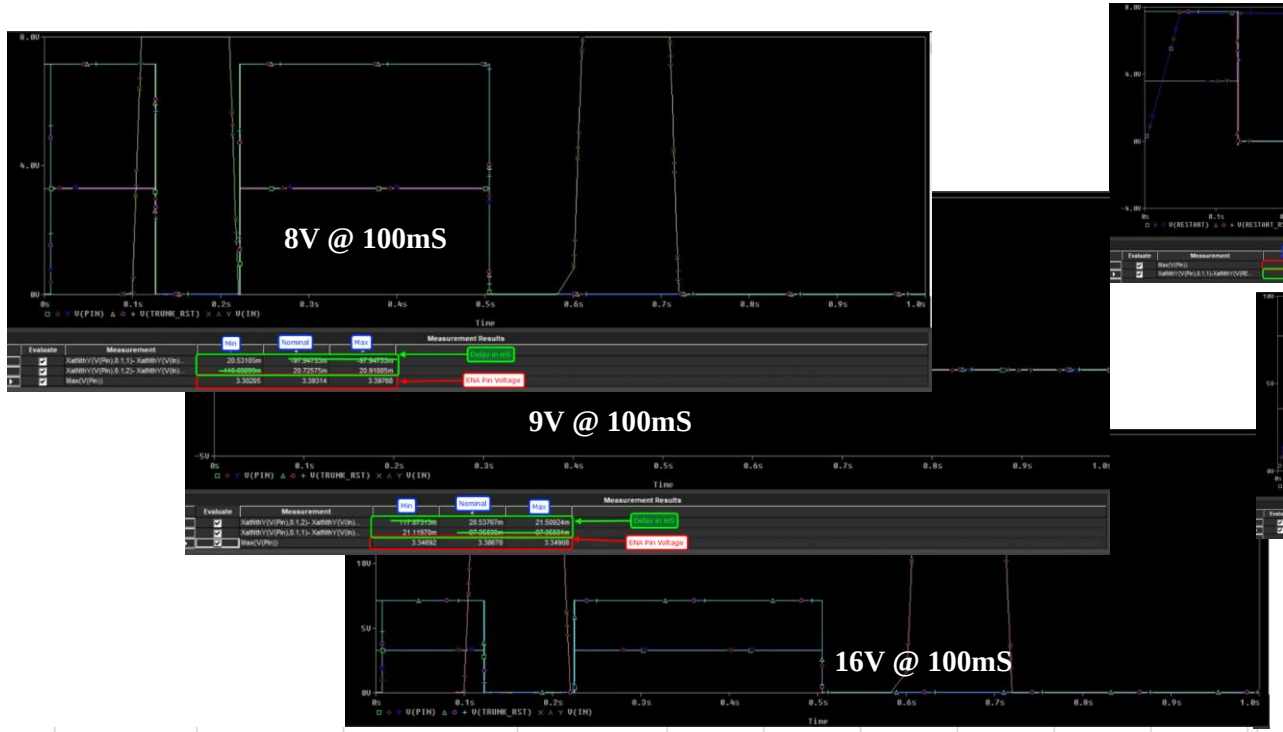
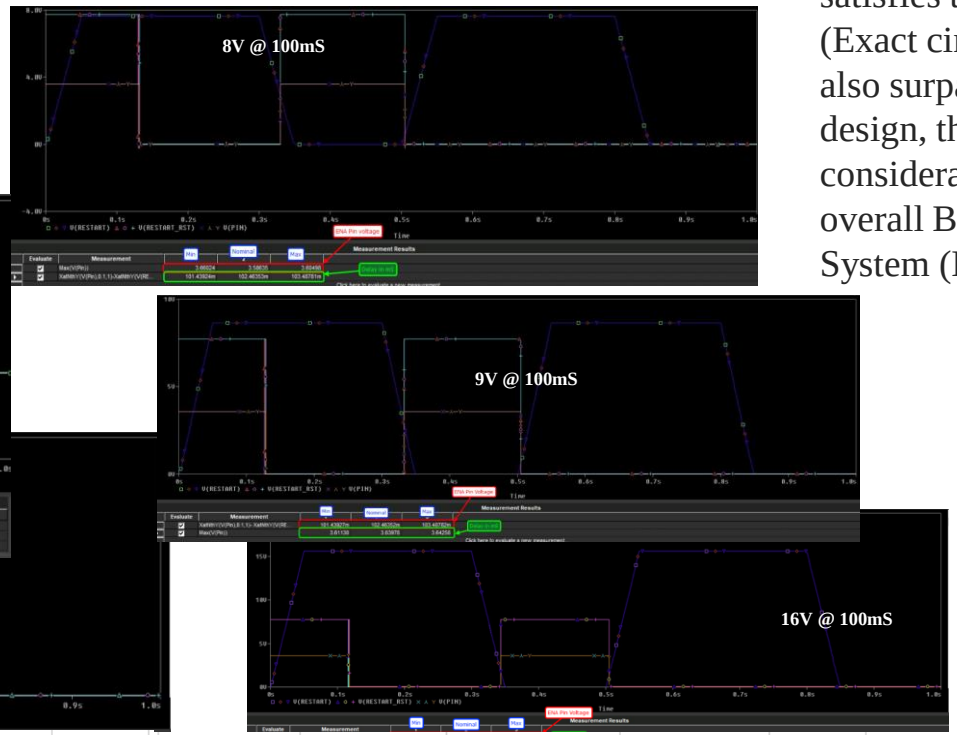
Proposed Design Result





Value Add's

This specific output not only satisfies their requirements (Exact circuit and delay) but also surpasses the Existing design, thereby adding considerable value to the overall Battery Management System (BMS).

Restart_W/up									
Vin(Volts)	Delay (mSec)			Vpin-R45/R46 (Volts)			VEna (Volts)		
Restart_W/up	Min C=792nF	Nominal C=800nF	Max C=808nF	Min	Nominal	Max	Min	Nominal	Max
8	101.43	102.46	103.46	3.66	3.58	3.6	3.491786	3.42053	3.444435
9	101.43	102.46	103.48	3.61	3.63	3.64	3.444084	3.468302	3.482802
16	101.43	102.46	103.48	3.61	3.59	3.67	3.444084	3.430084	3.511506

Trunk_W/up									
Vin(Volts)	Delay (mSec)			Vpin-R45/R46 (Volts)			VEna (Volts)		
Trunk_W/up	Min C=148.5nF	Nominal C=150nF	Max C=151.5nF	Min	Nominal	Max	Min	Nominal	Max
8	20.53	20.72	20.91	3.392	3.393	3.397	1.554173	1.565028	1.577224
9	21.1	20.53	21.5	3.346	3.386	3.349	1.563682	1.551424	1.586258
16	19.72	19.92	20.11	3.302	3.394	3.389	1.469151	1.521298	1.529632

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A Heartfelt Customer's Voice

I want to express my gratitude to GigHz for their outstanding work on our BMS module project. We faced a significant challenge with the existing circuit functionality on SBC1, which was not meeting our new requirements. GigHz not only addressed this issue promptly but also completed the entire project with remarkable efficiency. Their ability to deliver high-quality results within the specified time frame was impressive, providing a solution that not only met our new requirements but also did so at a low cost. The excellent performance of the redesigned circuit in the BMS module exceeded our expectations. I highly recommend GigHz for their expertise, commitment to excellence, and ability to overcome challenges.

Conclusion

- In summary, Despite the challenges create a hardware design, we created the complete circuit design along with analysis for worst circuit voltages.
- Provided the cost effective design without compromise in performance which makes the product design best suit the client requirement.
- With completing this design in short time period, marking a significant milestone in our journey.