Overvoltage Protection Circuit Modification in BMS

Scope: Hardware circuit Design

Application: Battery Management System

Effective management of rechargeable batteries relies heavily on the crucial hardware circuit design of a Battery Management System (BMS). Often considered the central intelligence of electric vehicles, the BMS ensures seamless operation. In particular, our focus lies in the hardware design of the Jumper (Overvoltage) Recognition section, where precision is essential. This section is tasked with recognizing overvoltage conditions, necessitating the accurate detection of press signals while filtering out sudden noise to prevent unintended execution of programmed tasks.

Challenges

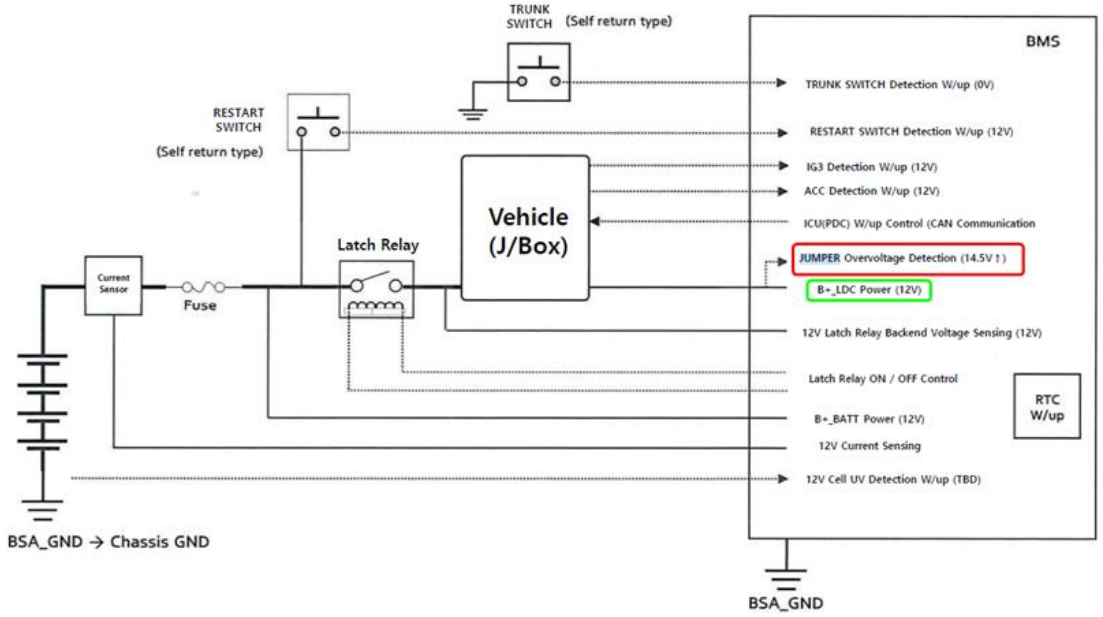
The client is facing a challenge with the existing design of the circuit on SBC1 within the BMS module, as it does not meet their below requirements.

Challenges:

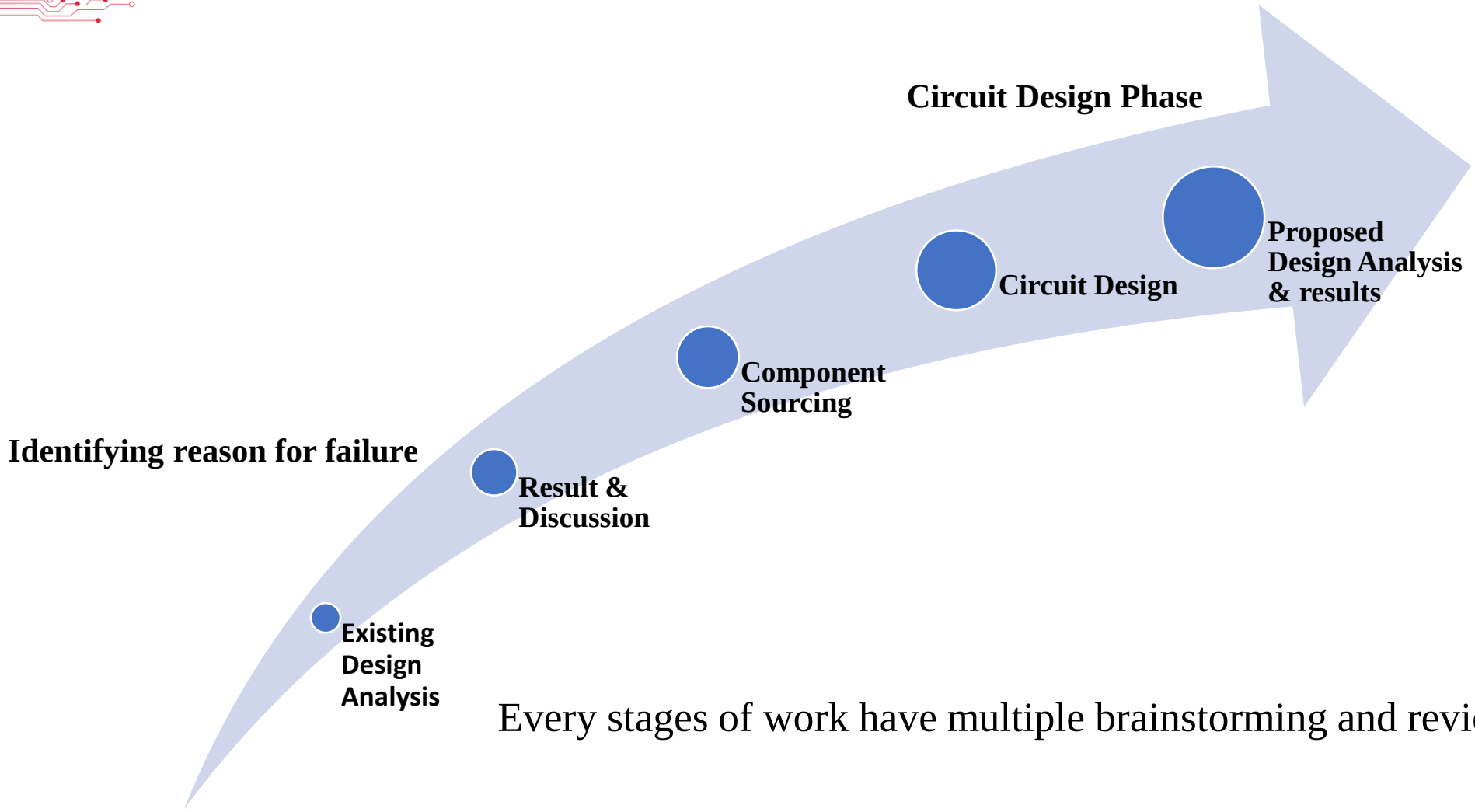
Wake up recognition:

For Jumper (Overcharge),

- Should be possible design by branching the internal pattern using the B+_LDC power pin
- Wake Up Recognition design
- Recognized as High from at least right before 14.5V and Wake up required
- Recognizing Off: Recognizing as Off up to 14V
- Check hysteresis characteristics for Wakeup recognition voltage



Hardware design-SoW

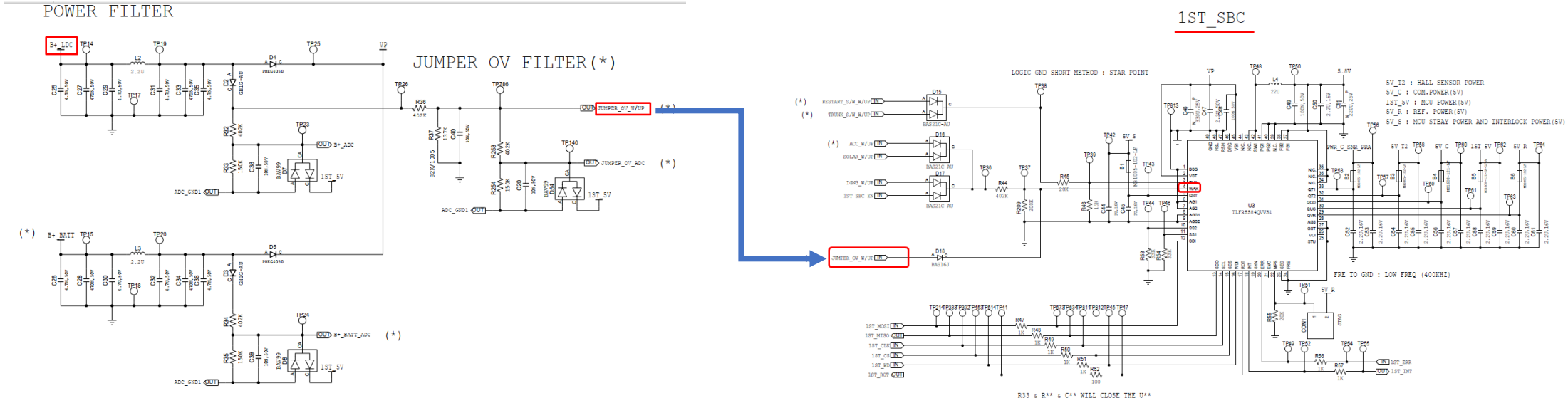


Every stages of work have multiple brainstorming and reviews with the client

Design Intent

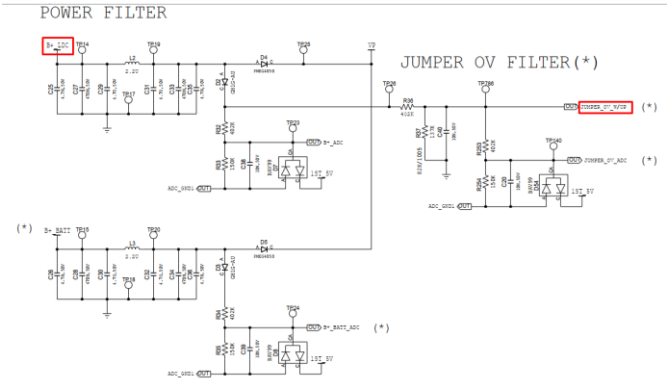
Design :Jumper (Over voltage Recognition)

The Jumper Circuit Design that identifies Overvoltage. If the input voltage (B+_LDC) is between 14 to 14.5V, the reset signal switches from high to low. This change allows the SBC to regulate the Power Management Integrated Circuit (PMIC) of this Battery Management System (BMS).



Identifying reason for failure

Existing Schematic

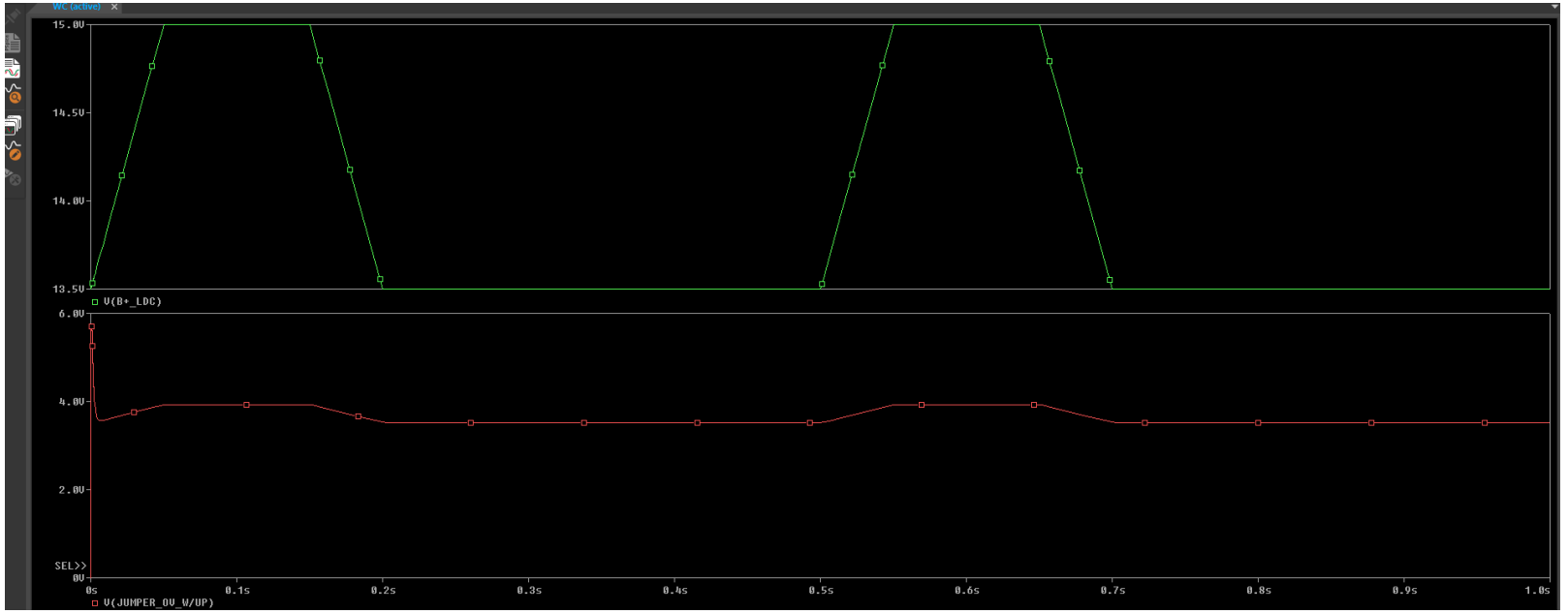


- The Jumper output signal is analog signal with sudden rise in voltage.
- So, SBC1 unable to use this signal for detect the Overvoltage recognition.

Existing Design Analysis

Existing Jumper Circuit Design consist a set of Discrete components to identify the Overvoltage.

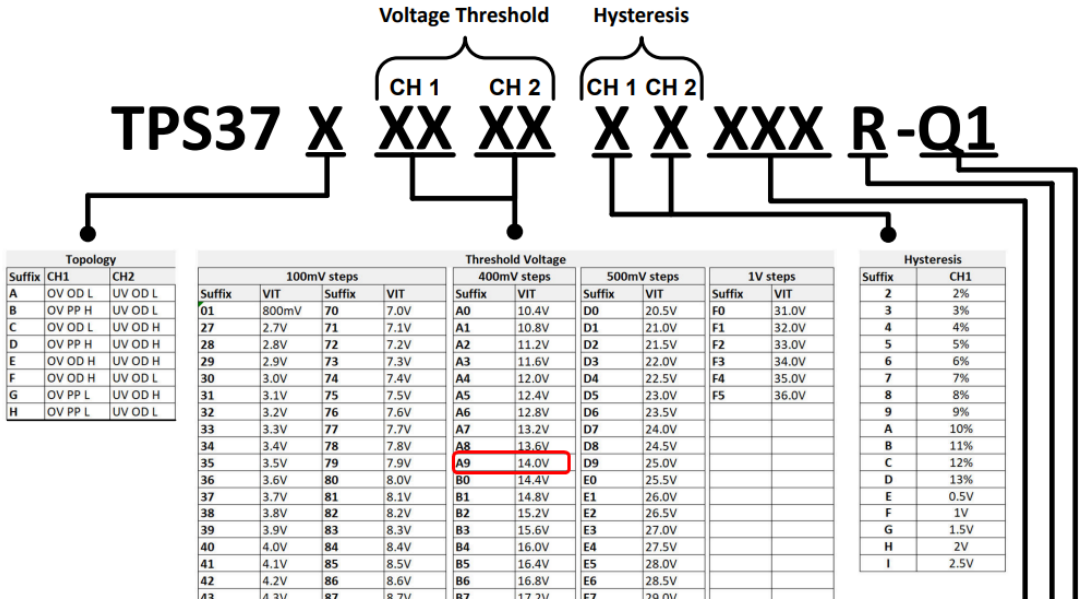
Existing Design Analysis output



Component Sourcing

Component Sourcing

- To rectify that existing issue, we planned to use Integrated chip instead of Discrete components for this particular voltage level.
- We sourced TI, Analog Devices and RoHM for component (IC).
- The IC-**TPS37AA90122DSKRQ1** from **TI** is configured to meet our design criteria by generating a reset output when the input voltage rises above **14V** in the circuit.



Topology

Suffix	CH1	CH2
A	OV OD L	UV OD L
B	OV PP H	UV OD L
C	OV OD L	UV OD H
D	OV PP H	UV OD H
E	OV OD H	UV OD H
F	OV OD H	UV OD L
G	OV PP L	UV OD H
H	OV PP L	UV OD L

Threshold Voltage

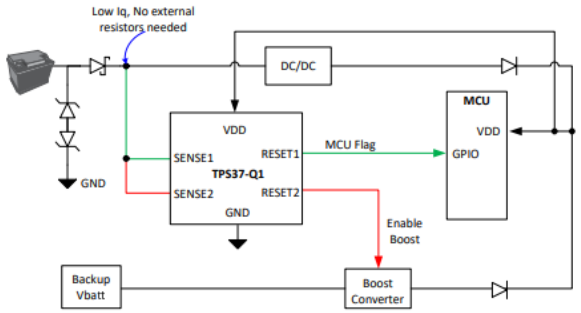
100mV steps				400mV steps		500mV steps		1V steps	
Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT
01	800mV	70	7.0V	A0	10.4V	D0	20.5V	F0	31.0V
27	2.7V	71	7.1V	A1	10.8V	D1	21.0V	F1	32.0V
28	2.8V	72	7.2V	A2	11.2V	D2	21.5V	F2	33.0V
29	2.9V	73	7.3V	A3	11.6V	D3	22.0V	F3	34.0V
30	3.0V	74	7.4V	A4	12.0V	D4	22.5V	F4	35.0V
31	3.1V	75	7.5V	A5	12.4V	D5	23.0V	F5	36.0V
32	3.2V	76	7.6V	A6	12.8V	D6	23.5V		
33	3.3V	77	7.7V	A7	13.2V	D7	24.0V		
34	3.4V	78	7.8V	A8	13.6V	D8	24.5V		
35	3.5V	79	7.9V	A9	14.0V	D9	25.0V		
36	3.6V	80	8.0V	B0	14.4V	E0	25.5V		
37	3.7V	81	8.1V	B1	14.8V	E1	26.0V		
38	3.8V	82	8.2V	B2	15.2V	E2	26.5V		
39	3.9V	83	8.3V	B3	15.6V	E3	27.0V		
40	4.0V	84	8.4V	B4	16.0V	E4	27.5V		
41	4.1V	85	8.5V	B5	16.4V	E5	28.0V		
42	4.2V	86	8.6V	B6	16.8V	E6	28.5V		

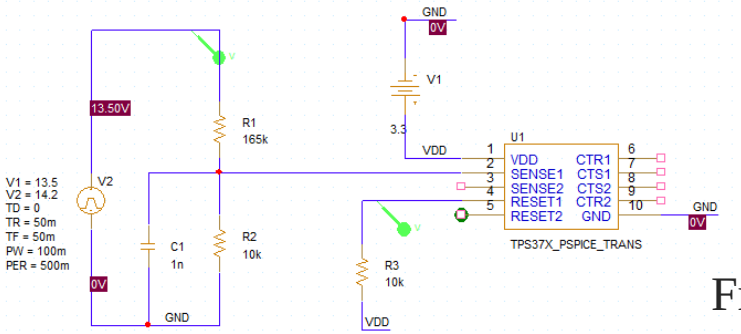
Hysteresis

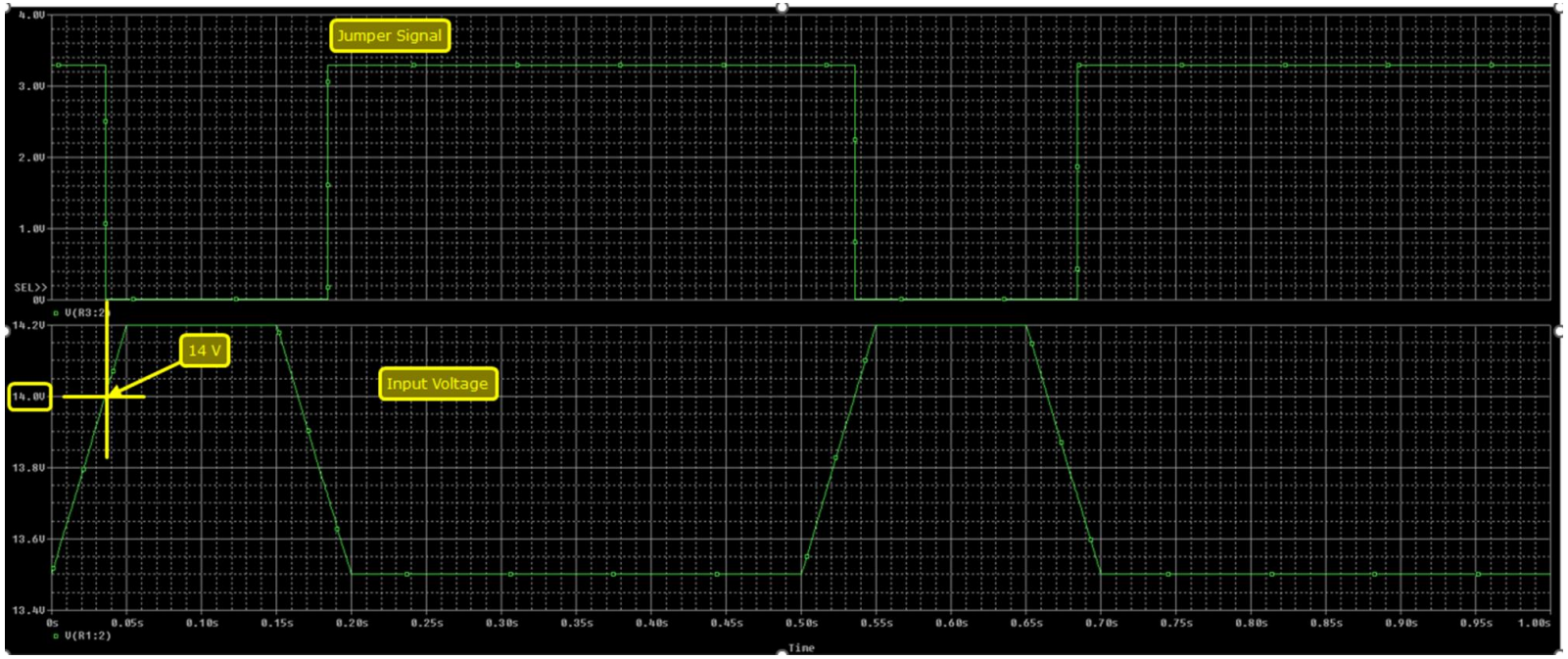
Suffix	CH1
2	2%
3	3%
4	4%
5	5%
6	6%
7	7%
8	8%
9	9%
A	10%
B	11%
C	12%
D	13%
E	0.5V
F	1V
G	1.5V
H	2V
I	2.5V

Circuit Design Phase

Created a rough schematic based on the application diagram to rough analysis to check the requirement and done an analysis to verify.







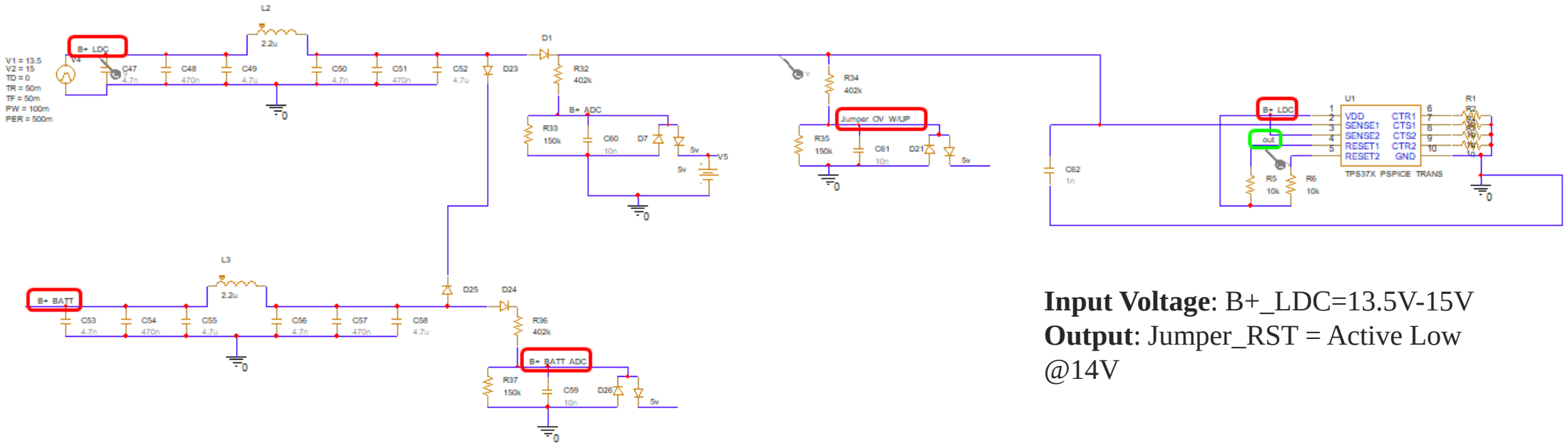
From the analysis of this IC , the reset signal is changed from High to Low, when the Input power reach the 14V.

Proposed Design

Proposed Design Analysis Setup

The analysis is done by simulating the Overvoltage circuit with configuration in IC (TPS37AA90122DSKRQ1).

Circuit Diagram

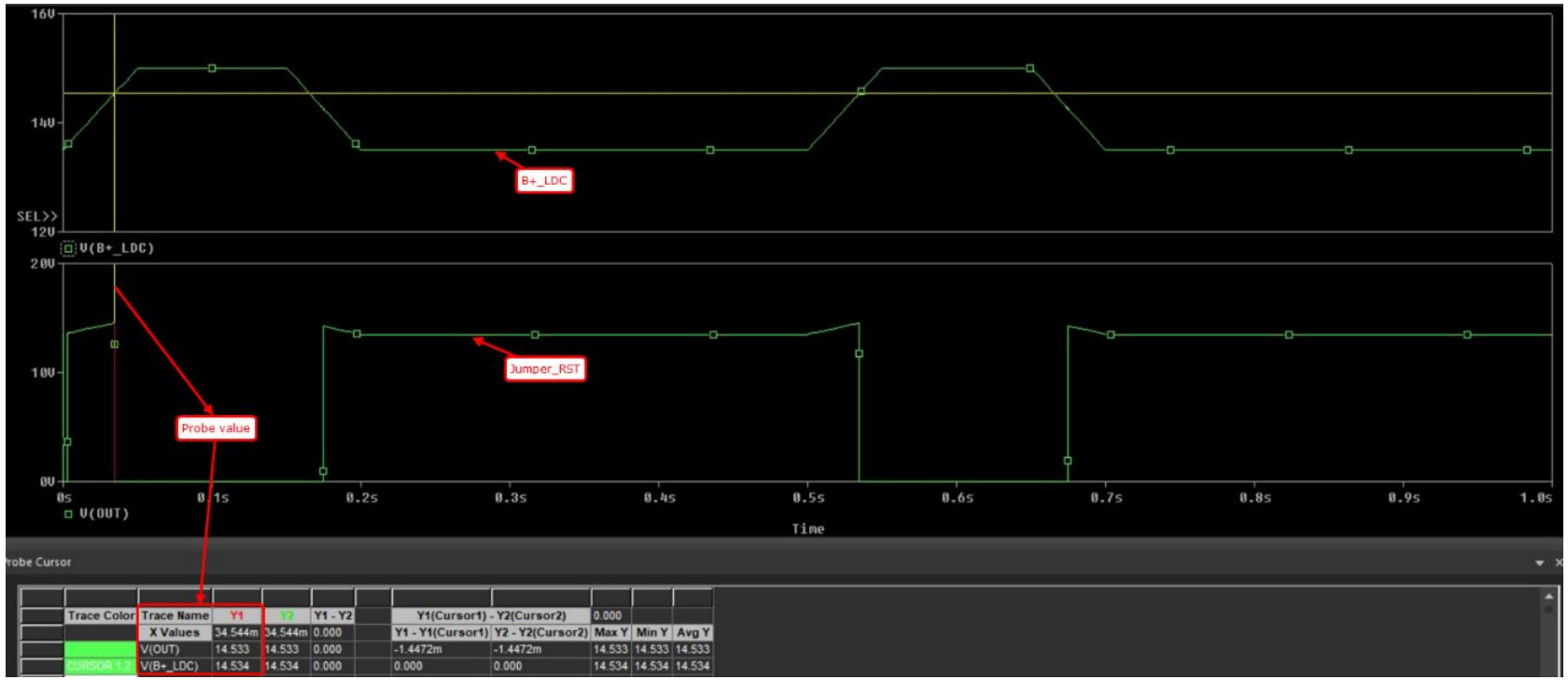


Input Voltage: B+_LDC=13.5V-15V
Output: Jumper_RST = Active Low @14V

Analysis and Result

Proposed Design Result

Reset output will be high at normal condition. When the input signal (B+_LDC) rises above 14V, the TPS37AA90122DSKRQ1 detects the overvoltage at 14.1V, making the Reset output low. This voltage is given at WAKE pin of SBC.



Input Voltage: B+_LDC=13.5V-15V
Output: Jumper_RST = Active Low @14V

Value add

This specific output not only satisfies their requirements but also surpasses the Existing design, thereby adding considerable value to the overall Battery Management System (BMS).

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"We are extremely satisfied with the remarkable performance of this exceptional team. Despite encountering numerous challenges, they adeptly crafted our circuit design, showcasing a seamless integration of creativity and expertise in their Engineering Services. What distinguishes them is their unwavering dedication to delivering a cost-efficient design without sacrificing quality. Within an unexpectedly brief timeframe, they not only fulfilled but surpassed our expectations, achieving a noteworthy milestone in our project. This team has demonstrated that they are the preferred choice for those in search of a winning blend of timeliness, affordability, and excellence.

Conclusion

- In summary, despite facing challenges, our team effectively designed the circuit through extensive brainstorming and utilizing our expertise in ECAD Engineering Services.
- We delivered a cost-effective design and outlined a quality-focused approach to create the circuit.
- Completing this design within a short timeframe marks a significant milestone in our journey.