

EDA Conversion for DMS Board

Scope: Electronic Design Automation Conversion

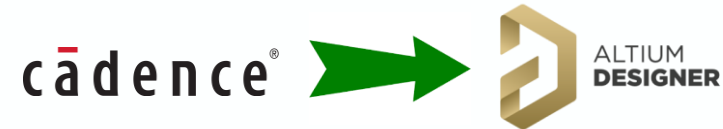
Application: Advanced Driver Assistance Systems

Our mission involves the transformation of Printed Circuit Board (PCB) files for the Driver Monitoring System (DMS) from Cadence to Altium Designer via EDA conversion. DMS is a technology embedded in modern car systems to observe and analyze the driver's actions, focus, and general state. Using sensors and cameras, the system tracks facial features, eye movements, and behavior. This data is analyzed to determine the driver's alertness level, issuing alerts or interventions if signs of drowsiness, distraction, or safety concerns are identified.



Challenges

We were tasked with converting their PCB files from Cadence to Altium Designer.

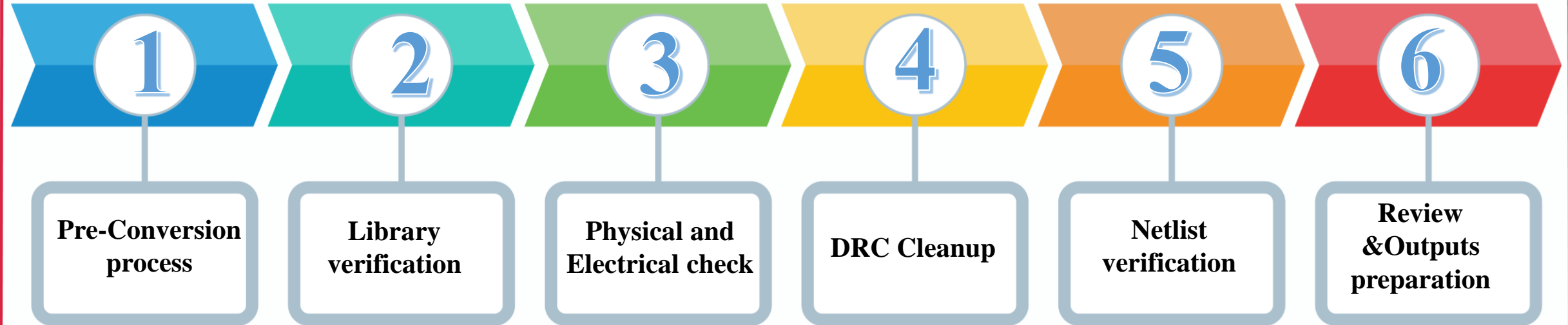


Challenges:

- Attain 99.99% physical accuracy in the Altium design compared to the provided design file
- Achieve a 100% electrical match between the converted Altium design and the provided design file.
- Contains lot of Length Matching Groups
- To match the exact Footprint Libraries (Pad's Round Corners)
- Netlist syncing up



EDA Conversion-SoW



Pre-Conversion Process

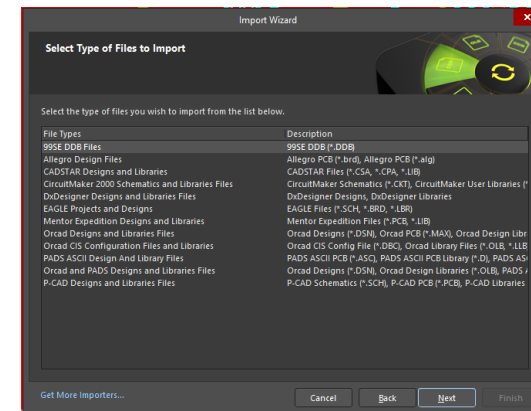
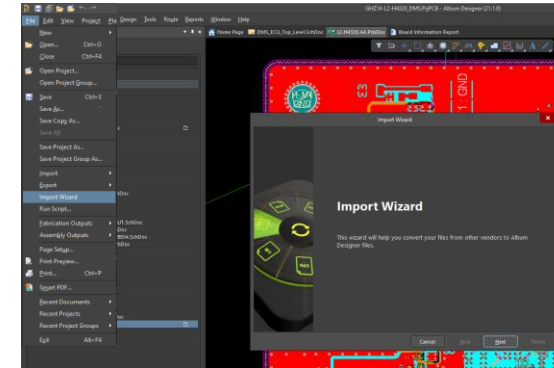
- Pre conversion verification:**

- Prepare and Review the cadence files as per the formats for Altium conversion.

	Cadence	Altium
Schematic File	.dsn	.schdoc
PCB File	.brd	.pcbdoc

Import to the Altium:

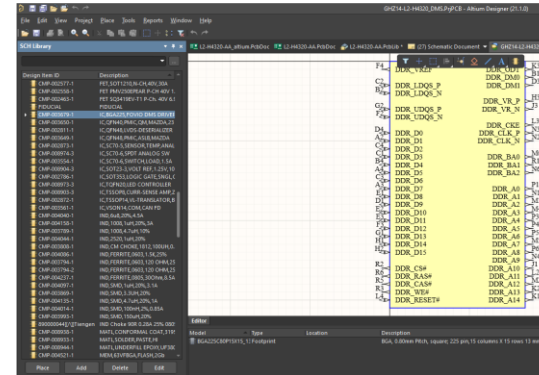
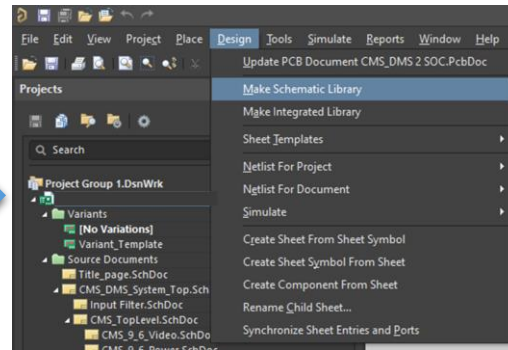
- Schematic and PCB Conversion in Altium designer



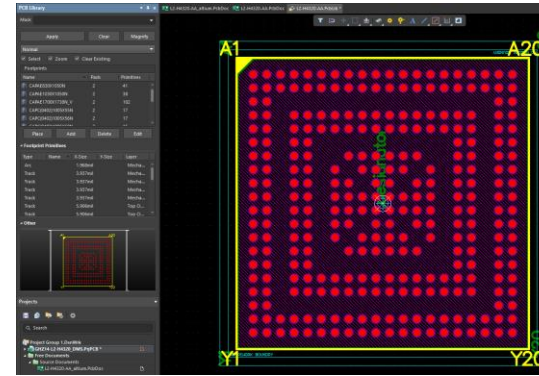
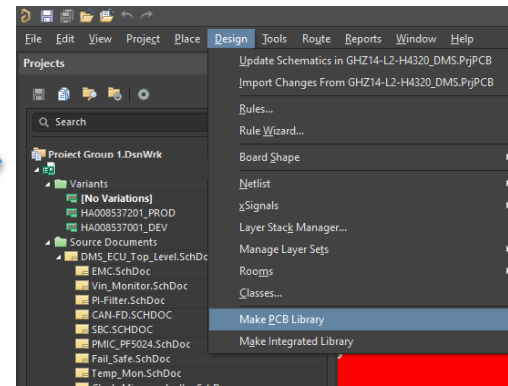
Library verification

- Creating Symbol and Footprint Libraries from the Schematics and PCB Layout
- Library Verifications and modifying as per Standards
- Physical and Electrical comparison of Libraries

Schematic Library

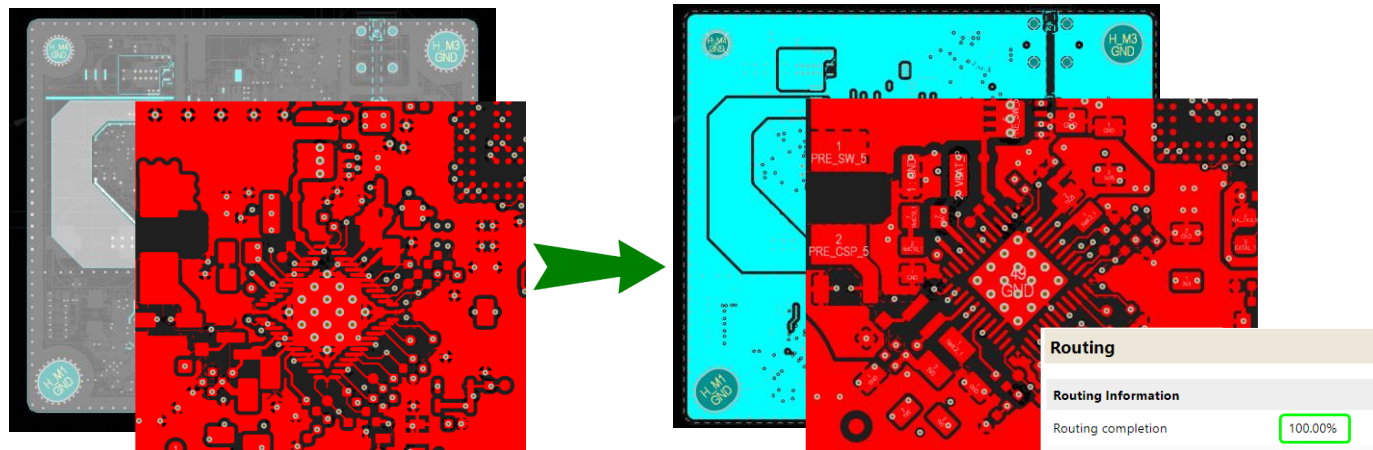
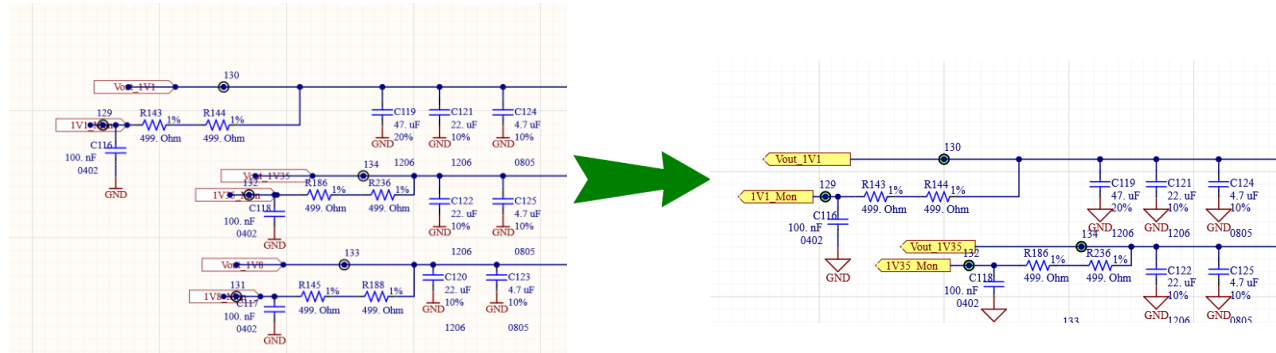


PCB Library



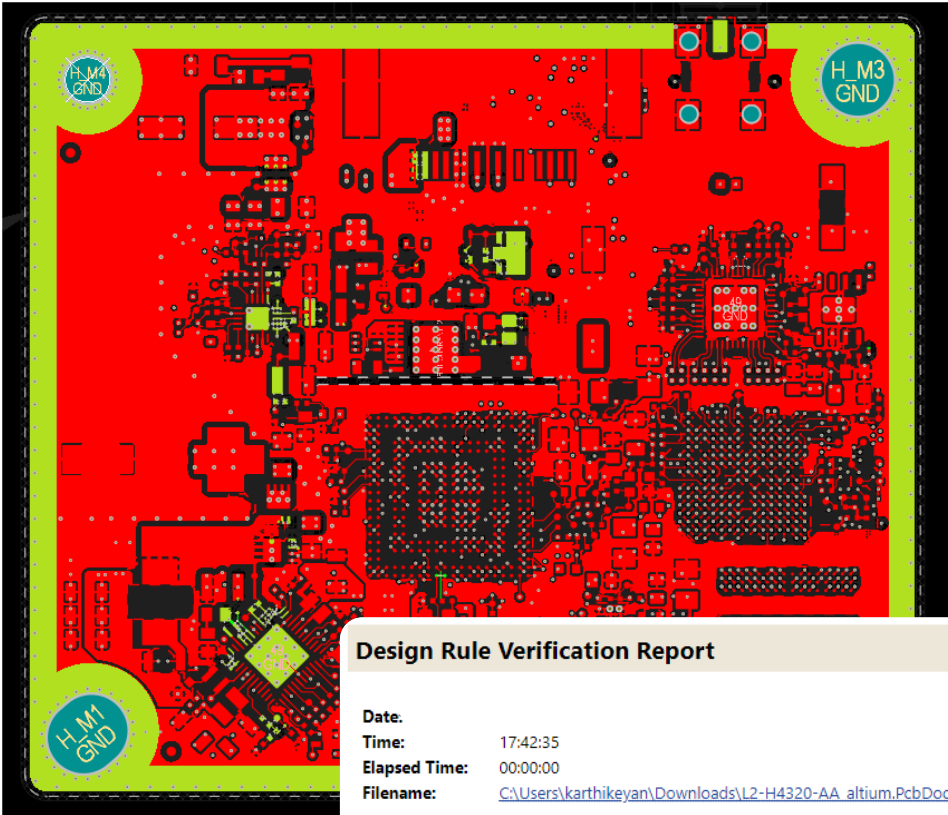
Physical & Electrical Check

- Physical and Electrical comparison of Schematics & PCB Layout and Error and Physical Clean up in both schematics and PCB Layout.



DRC Clean up

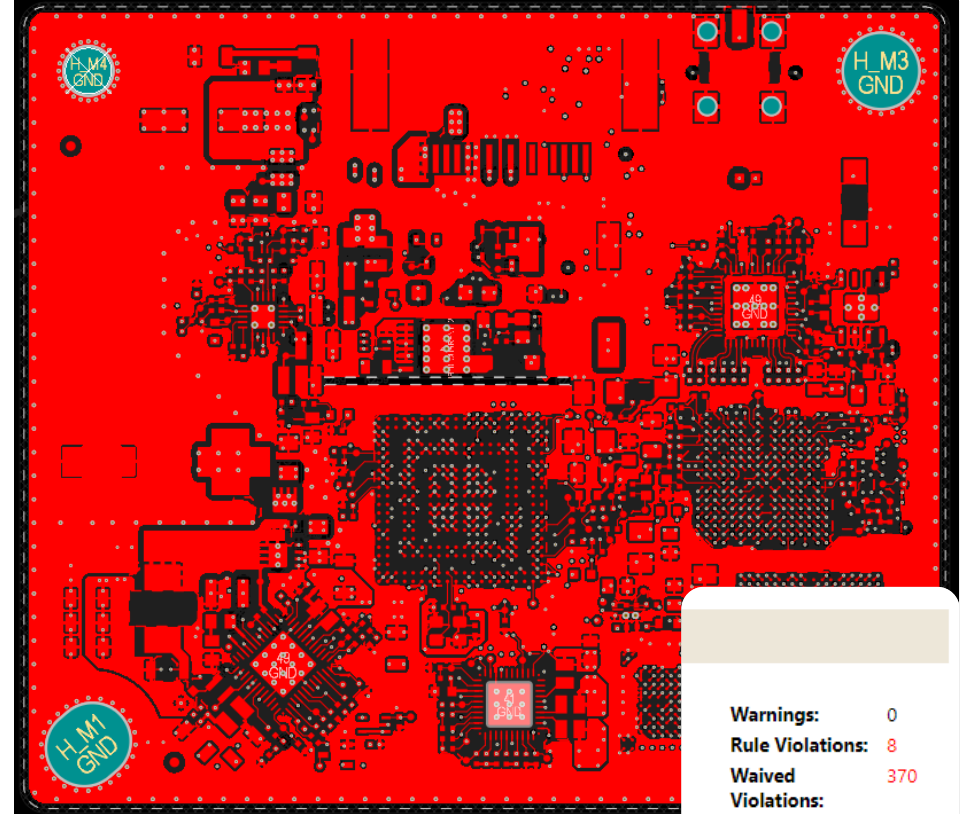
➤ Define rules and DRC clean up



Design Rule Verification Report

Date: 17:42:35
Time: 17:42:35
Elapsed Time: 00:00:00
Filename: C:\Users\karthikeyan\Downloads\L2-H4320-AA_altium.PcbDoc_2023-11-29.pcbdoc

ERROR : More than 500 violations detected, DRC was stopped



Warnings: 0
Rule Violations: 8
Waived Violations: 370

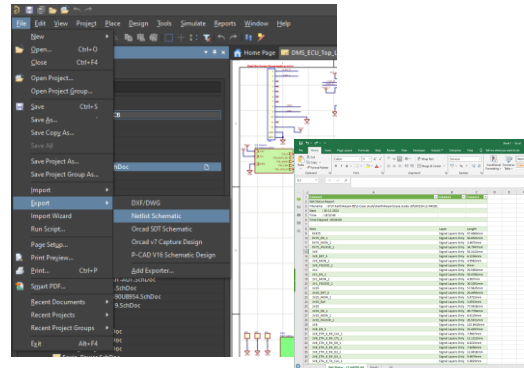
Netlist Verification

- Generate a netlist in Altium Designer and then proceed to compare it with the netlist provided by the client.

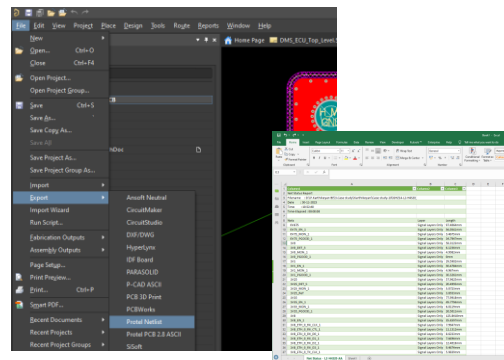
Netlist generation in Altium

Netlist From Client

Schematic Netlist



PCB Netlist



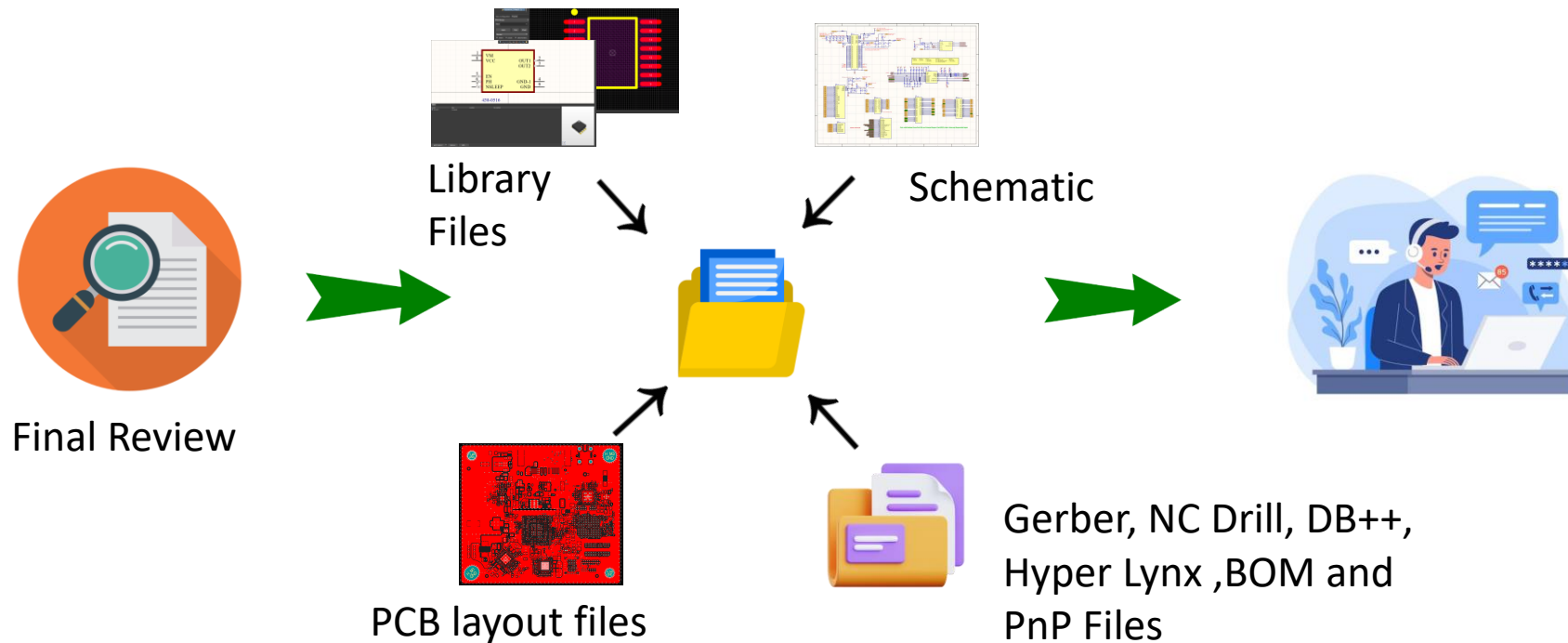
Component	Value	Location
U1	74VHC00	U1
U2	74VHC00	U2
U3	74VHC00	U3
U4	74VHC00	U4
U5	74VHC00	U5
U6	74VHC00	U6
U7	74VHC00	U7
U8	74VHC00	U8
U9	74VHC00	U9
U10	74VHC00	U10
U11	74VHC00	U11
U12	74VHC00	U12
U13	74VHC00	U13
U14	74VHC00	U14
U15	74VHC00	U15
U16	74VHC00	U16
U17	74VHC00	U17
U18	74VHC00	U18
U19	74VHC00	U19
U20	74VHC00	U20
U21	74VHC00	U21
U22	74VHC00	U22
U23	74VHC00	U23
U24	74VHC00	U24
U25	74VHC00	U25
U26	74VHC00	U26
U27	74VHC00	U27
U28	74VHC00	U28
U29	74VHC00	U29
U30	74VHC00	U30
U31	74VHC00	U31
U32	74VHC00	U32
U33	74VHC00	U33
U34	74VHC00	U34
U35	74VHC00	U35
U36	74VHC00	U36
U37	74VHC00	U37
U38	74VHC00	U38
U39	74VHC00	U39
U40	74VHC00	U40
U41	74VHC00	U41
U42	74VHC00	U42
U43	74VHC00	U43
U44	74VHC00	U44
U45	74VHC00	U45
U46	74VHC00	U46
U47	74VHC00	U47
U48	74VHC00	U48
U49	74VHC00	U49
U50	74VHC00	U50
U51	74VHC00	U51
U52	74VHC00	U52
U53	74VHC00	U53
U54	74VHC00	U54
U55	74VHC00	U55
U56	74VHC00	U56
U57	74VHC00	U57
U58	74VHC00	U58
U59	74VHC00	U59
U60	74VHC00	U60
U61	74VHC00	U61
U62	74VHC00	U62
U63	74VHC00	U63
U64	74VHC00	U64
U65	74VHC00	U65
U66	74VHC00	U66
U67	74VHC00	U67
U68	74VHC00	U68
U69	74VHC00	U69
U70	74VHC00	U70
U71	74VHC00	U71
U72	74VHC00	U72
U73	74VHC00	U73
U74	74VHC00	U74
U75	74VHC00	U75
U76	74VHC00	U76
U77	74VHC00	U77
U78	74VHC00	U78
U79	74VHC00	U79
U80	74VHC00	U80
U81	74VHC00	U81
U82	74VHC00	U82
U83	74VHC00	U83
U84	74VHC00	U84
U85	74VHC00	U85
U86	74VHC00	U86
U87	74VHC00	U87
U88	74VHC00	U88
U89	74VHC00	U89
U90	74VHC00	U90
U91	74VHC00	U91
U92	74VHC00	U92
U93	74VHC00	U93
U94	74VHC00	U94
U95	74VHC00	U95
U96	74VHC00	U96
U97	74VHC00	U97
U98	74VHC00	U98
U99	74VHC00	U99
U100	74VHC00	U100

Component	Value	Location
U1	74VHC00	U1
U2	74VHC00	U2
U3	74VHC00	U3
U4	74VHC00	U4
U5	74VHC00	U5
U6	74VHC00	U6
U7	74VHC00	U7
U8	74VHC00	U8
U9	74VHC00	U9
U10	74VHC00	U10
U11	74VHC00	U11
U12	74VHC00	U12
U13	74VHC00	U13
U14	74VHC00	U14
U15	74VHC00	U15
U16	74VHC00	U16
U17	74VHC00	U17
U18	74VHC00	U18
U19	74VHC00	U19
U20	74VHC00	U20
U21	74VHC00	U21
U22	74VHC00	U22
U23	74VHC00	U23
U24	74VHC00	U24
U25	74VHC00	U25
U26	74VHC00	U26
U27	74VHC00	U27
U28	74VHC00	U28
U29	74VHC00	U29
U30	74VHC00	U30
U31	74VHC00	U31
U32	74VHC00	U32
U33	74VHC00	U33
U34	74VHC00	U34
U35	74VHC00	U35
U36	74VHC00	U36
U37	74VHC00	U37
U38	74VHC00	U38
U39	74VHC00	U39
U40	74VHC00	U40
U41	74VHC00	U41
U42	74VHC00	U42
U43	74VHC00	U43
U44	74VHC00	U44
U45	74VHC00	U45
U46	74VHC00	U46
U47	74VHC00	U47
U48	74VHC00	U48
U49	74VHC00	U49
U50	74VHC00	U50
U51	74VHC00	U51
U52	74VHC00	U52
U53	74VHC00	U53
U54	74VHC00	U54
U55	74VHC00	U55
U56	74VHC00	U56
U57	74VHC00	U57
U58	74VHC00	U58
U59	74VHC00	U59
U60	74VHC00	U60
U61	74VHC00	U61
U62	74VHC00	U62
U63	74VHC00	U63
U64	74VHC00	U64
U65	74VHC00	U65
U66	74VHC00	U66
U67	74VHC00	U67
U68	74VHC00	U68
U69	74VHC00	U69
U70	74VHC00	U70
U71	74VHC00	U71
U72	74VHC00	U72
U73	74VHC00	U73
U74	74VHC00	U74
U75	74VHC00	U75
U76	74VHC00	U76
U77	74VHC00	U77
U78	74VHC00	U78
U79	74VHC00	U79
U80	74VHC00	U80
U81	74VHC00	U81
U82	74VHC00	U82
U83	74VHC00	U83
U84	74VHC00	U84
U85	74VHC00	U85
U86	74VHC00	U86
U87	74VHC00	U87
U88	74VHC00	U88
U89	74VHC00	U89
U90	74VHC00	U90
U91	74VHC00	U91
U92	74VHC00	U92
U93	74VHC00	U93
U94	74VHC00	U94
U95	74VHC00	U95
U96	74VHC00	U96
U97	74VHC00	U97
U98	74VHC00	U98
U99	74VHC00	U99
U100	74VHC00	U100



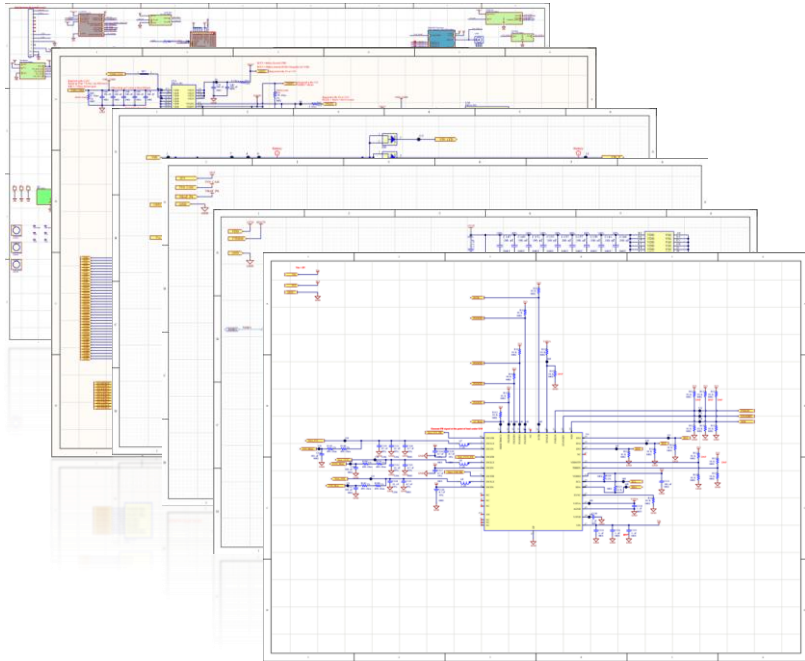
Review & Outputs

- Data syncing up (Combining schematic and PCB as project)
- Final Review compare with original file and Output files Preparation for Deliverables



Results-In Altium Designer

Schematics



PCB layout



EDA conversion of Cadence to Altium designer results that matched electrically by 100% and Physically by 99.99%



Client Testimonial

Offered is a testimonial from a delighted client, serving as compelling evidence of the Effectiveness of EDA Conversion.

"Working with GigHz was a transformative experience. Their seamless conversion of our PCB design files from Cadence to Altium Designer showcased a rare blend of efficiency, precision, and dedication. They delivered within the agreed timeframe, offering cost-effective solutions that perfectly aligned with our budget constraints. The quality of their work, evident in the meticulous attention to detail and flawless execution, exceed our expectations. GigHz is a testament to a harmonious balance of time efficiency, cost-effectiveness, and uncompromised quality - an invaluable partner for anyone navigating the complexities of electronic design and PCB development."



Conclusion

We demonstrated our commitment to excellence and technical expertise by delivering EDA conversion and results that precisely matched with Client's requirements.

Our collaboration integrates expertise with personalized service, alongside technical proficiency.

Our dedication is evident in the provision of top-notch EDA conversion PCB layouts, not only cutting costs but also highlighting our capability and dependability in consistently achieving outstanding results. Emphasizing quality and adhering to timelines are central to our approach.

