



Autodimming Retro Vision Mirrors

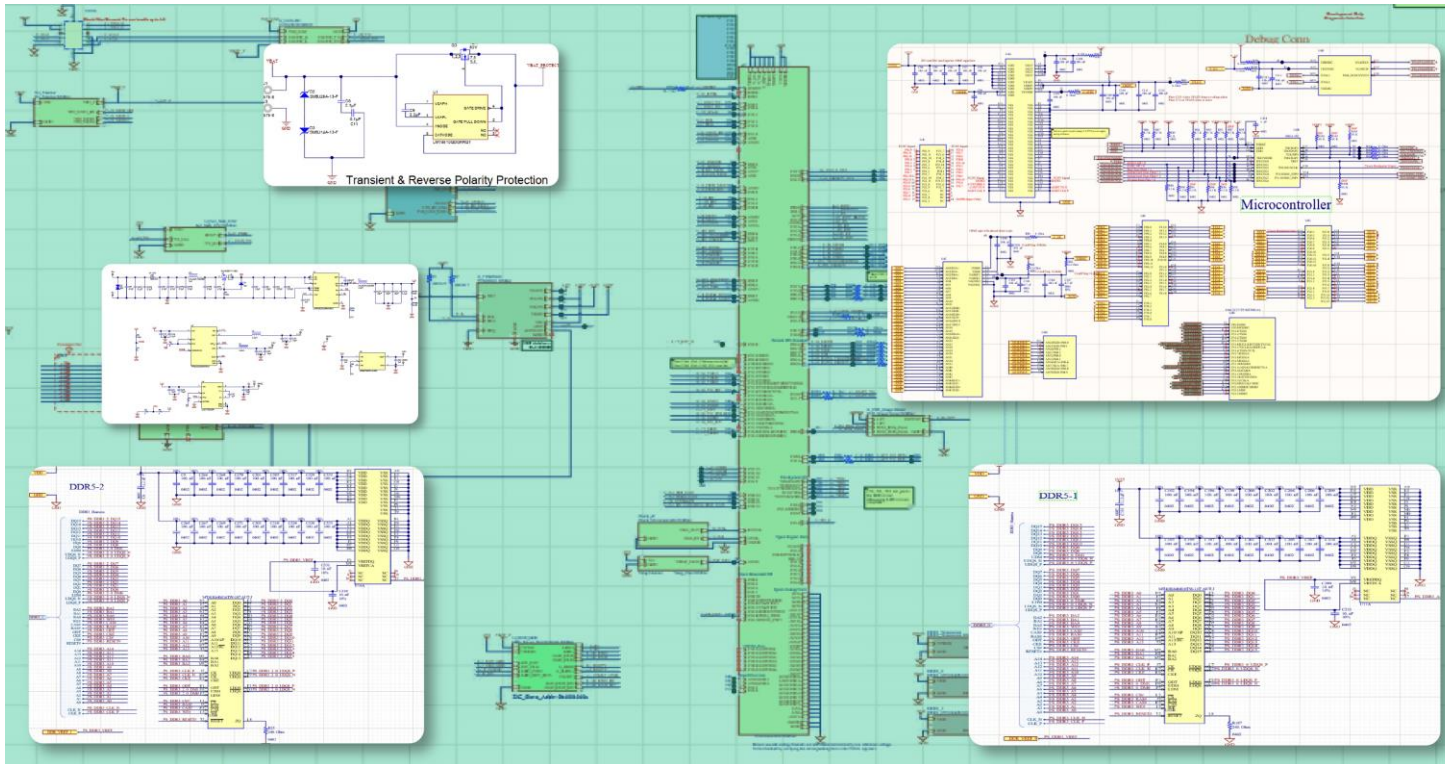
Scope: End-End PCB Design with Analysis

Application: ADAS

The Autodimming RetroVision Mirror is an intelligent automotive rearview mirror that automatically adjusts its brightness in response to glare from headlights. It reduces blinding effects, enhancing safety during nighttime driving. Using electrochromic technology or gel-based systems, sensors detect light intensity and darken the mirror to reduce glare. This feature is seamless and effortless for drivers, reducing eye strain and maintaining focus on the road. A valuable safety feature that enhances driving comfort and safety.



• Schematics



• PCB

- Total components → 1087
- Layer count → 10
- Total connection → 2493
- Pin count: 3184
- Devices → SOC (XA Zynq-7000 SoC), DDR4(x2), Flash, Microcontroller, Ethernet, Light sensor, CAN Transceiver, SBC, PMIC, LED Driver, Buck Converter, LDO, Load Switch, Regulators.

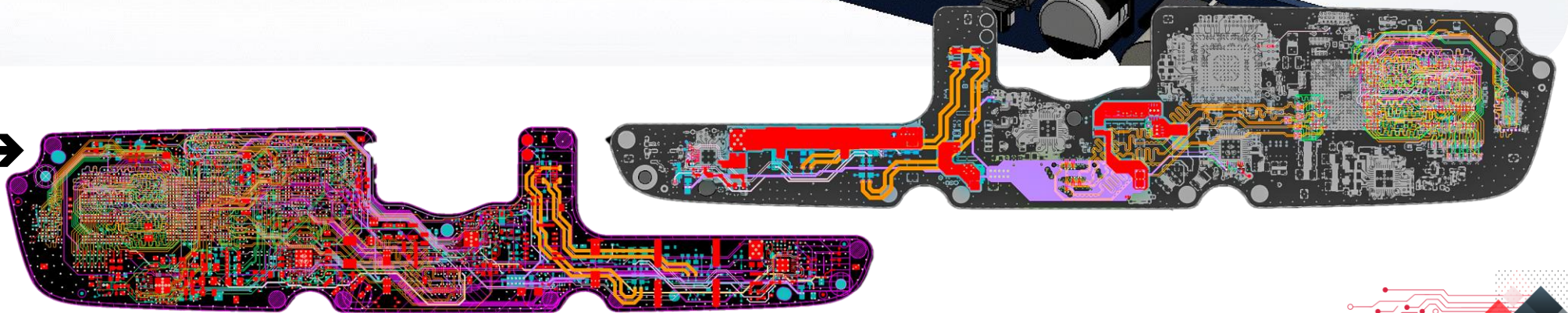


Challenges in PCB

- Interface:
- DDR4, CSI, I2C, MDI, NOR, UART, USB, advanced image sensor pipeline (ISP), JTAG
- Contains 13 different Powers
- High Speed signals with GND reference
- BGA Pitch – 0.8mm

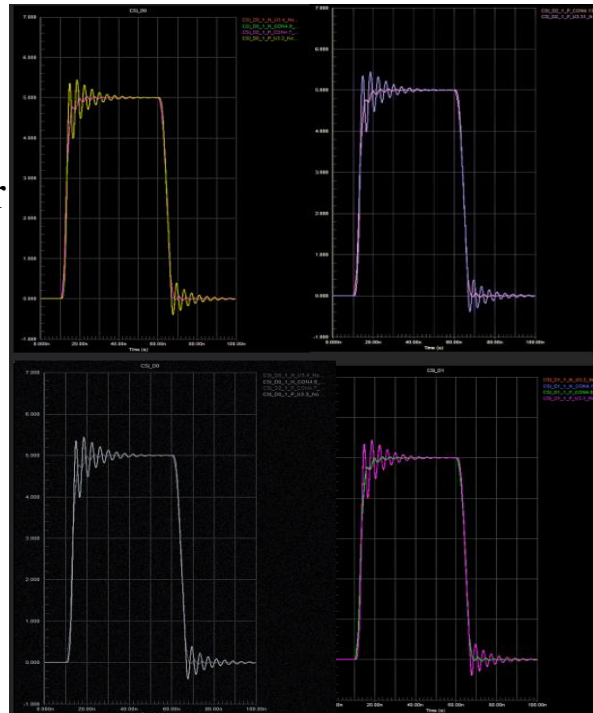


- Output →

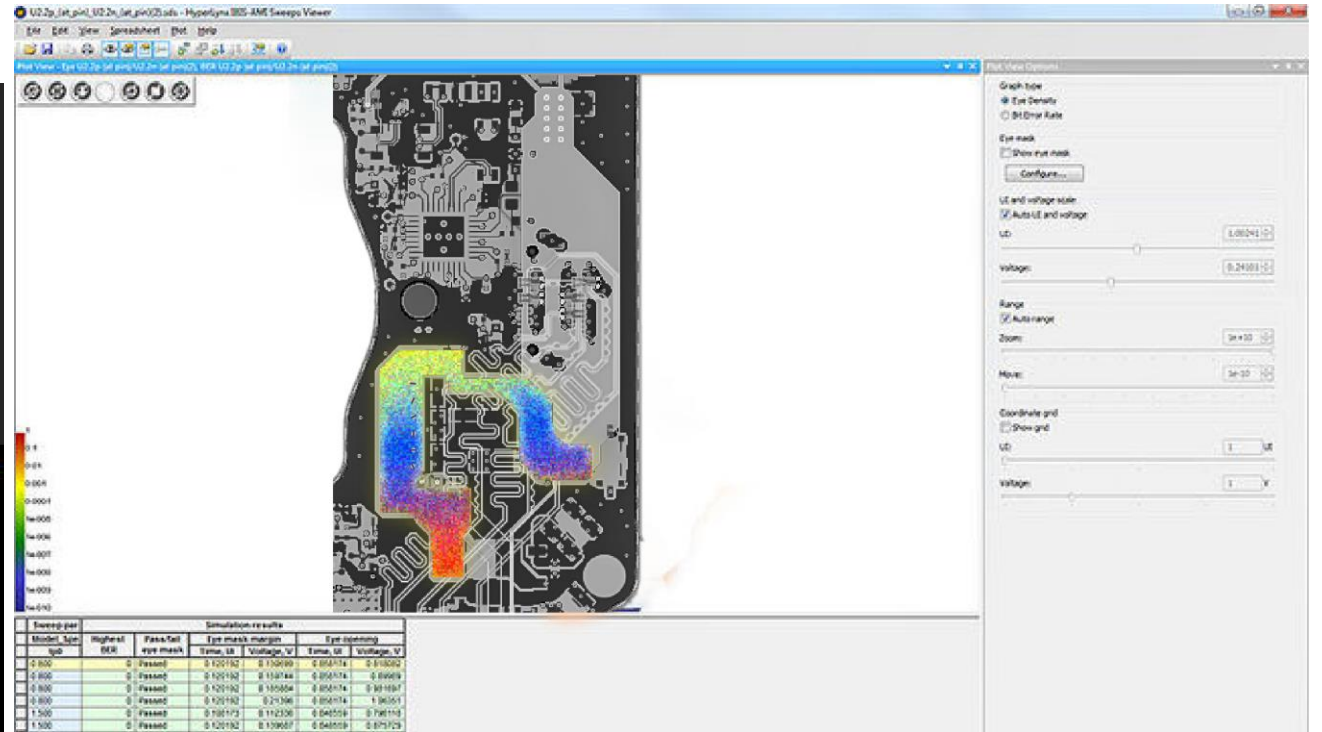


Analysis

- SI
- Tool – HyperLynx
- Checked for Overshoot in CSI signal
- CSI – 5 Signal Pairs
- Result:
- The Overshoot under acceptable limit



- PI
- Tool – HyperLynx



Analysis

- WCCA
- Tool – PSpice
- Checked for the time taken by the LDO to reach within required time even in Worst Condition.
- Result:
- From the theoretical and practical result it is within it's required limit.

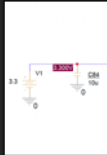
Working-Circuit Operation

The LDO makes use of bypass component in this function crucial role. To maintain proper non-overlapping internal capacitor. In the first phase (S1 and S2 transistor switches and charging capacitor. In the second phase (S3 and S4) the capacitor discharges between the input and output.

LDO to reach its output value extreme conditions. So, the LDO operates efficiently because of the CAN transceiver.

Design Goal: Time taken by

PSpice schematics



Input Probe: V(C85:2)

Output Probe: V(C87:2)

Calculation:

$$R_{OUT} = 2 \cdot R_{SW} + \frac{1}{F_{SW} \times C_1} + 4 \cdot ESR_{C1} + E_{C1}$$

$$t = 5\tau = 5R_{equiv}C_{ext} = \frac{5C_0}{C_{int}F_0}$$

Based on the formulas provided, the time required for the Output(5V) regulator in this project.

Need of WCCA

It is crucial for the power transceiver to operate properly dependent on the output voltage. The time it takes for the LDO to reach its output voltage is crucial for the CAN transceiver, as it serves as

CALCULATION:

$$t = 5\tau = 5R_{OUT}C_{OUT}$$

$$R_{OUT} = 2 \cdot R_{SW} + \frac{1}{F_{SW} \times C_1} + 4 \cdot ESR_{C1} + E_{C1}$$

FOR THIS CIRCUIT,

$$R_{SW} = 3\Omega, C_1 = 1\mu F, C_{OUT} = 2.2\mu F$$

$$F_{SW} = 2MHz$$

$$R_{OUT} = 2 \cdot R_{SW} + \frac{1}{F_{SW} \times C_1} + 4 \cdot ESR_{C1} + E_{C1}$$

$$= 2(3) + \frac{1}{2 \times 10^6 \times 1 \times 10^{-6}} + 4(0.01) + 0.01$$

$$= 6 + \frac{1}{2} = 6.5\Omega$$

$$R_{OUT} = 6.5\Omega$$

$$t = 5\tau = 5R_{OUT}C_{OUT}$$

$$= 5(6.5)(2.2 \times 10^{-6})$$

$$= 71.5 \times 10^{-6}$$

$$t = 71.5 \mu S$$

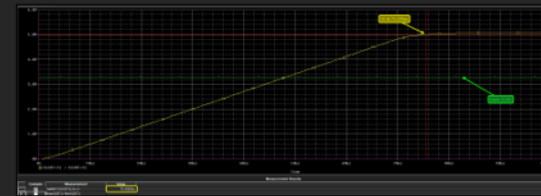
So, from this above calculation, the Output voltage will reach 5V in 71.5μs.

Simulation Graphs

At, X-axis: Time

At, Y-axis: Voltage (LDO's Output)

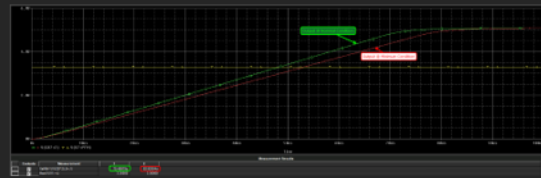
Time Vs Voltage Plot at Nominal Condition



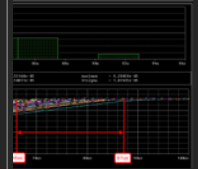
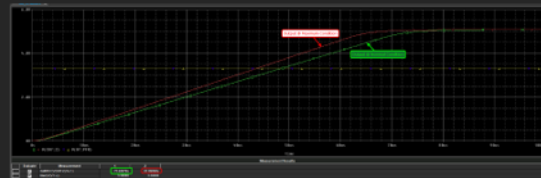
So, from the Simulation, at 75.43938 μs the LDO reach 5V.

From the calculation the time is 71.5μs.

Time Vs Voltage Plot at Minimum Condition



Time Vs Voltage Plot at Maximum Condition



Time of 5V is achieved in due

MIN (Extreme LOW)
82.92554 μs

Time taken between from 66μs to

It has been confirmed that the circuit will operate within the specified time to assert that the circuit

500 S02 - CMS GEN3



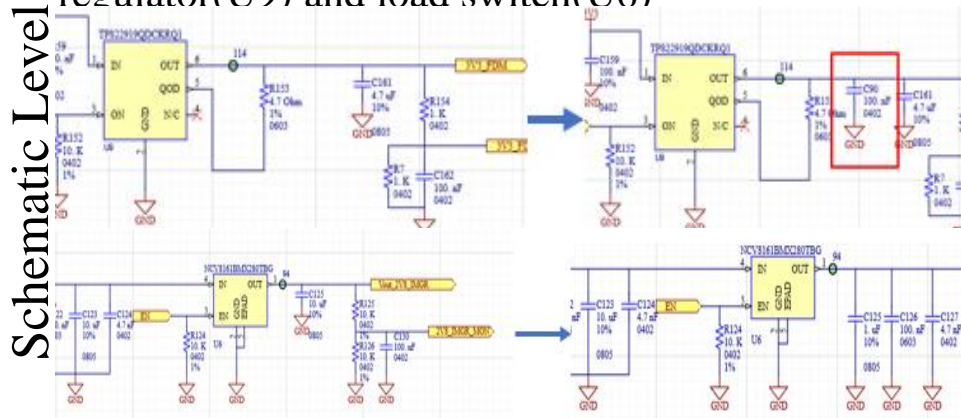
EMI/EMC

The conducted and radiated RF test is conducted in the board to identify the EMI/EMC problems.



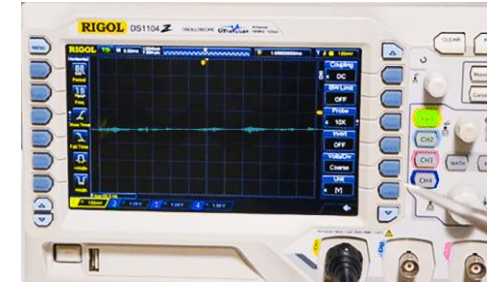
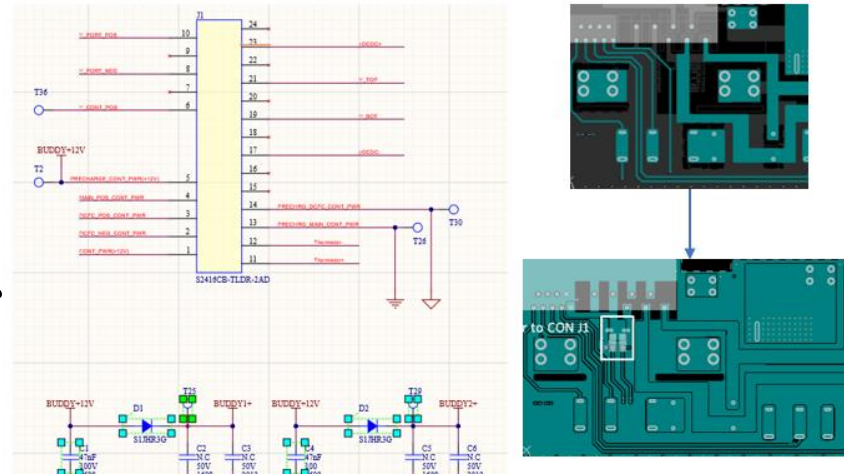
Figure shows failed measure signal where Noise occurred at output data.

Suggests to add 100nF Capacitor to the output pin of regulator(U9) and load switch(U6)



Power net (+12V) components placed closer to CON J1 as shown below.

Layout Level



After implementing this minor correction, the results obtained look truly remarkable



Outsourcing

- Here is a testimonial from a satisfied customer that serves as compelling evidence for the success of outsourcing PCB design

Outsourcing PCB design has been a transformative decision for us.

With access to a global talent pool, we've received high-quality designs at a cost-effective rate.

The seamless collaboration with offshore teams saved us time and resources, delivering exceptional results.

Our PCB design capabilities have been elevated, giving us a competitive edge in the market.

" We highly recommend outsourcing for those seeking success in their engineering projects."

Tier 1 Automotive Supplier North America



Conclusion

- Elevate your electronics to new heights with our expert PCB design services.
- Trust in our precise innovative passion for crafting cutting-edge circuitry. Let us bring your visions to life and optimize your technology for success.
- Experience the future of innovation with our unparalleled design expertise.
- By providing end-to-end solutions, we assist clients in realizing efficient and reliable through our analysis result to produce the finest PCB end product.
- With precision as our compass, we craft designs that stand the test of time. Our focus on quality ensures excellence in every aspect of our work.

Your satisfaction is our priority!

